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Slew-rate enhancement and trojan state avoiding for fully-differential operational amplifier

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Slew-rate enhancement and trojan state avoiding for fully-differential operational amplifier

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DEDICATION

To my parents

TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

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ABSTRACT

Operational amplifiers are fundamental building blocks in modern analog and mixed-signal systems such as data converters, switched-capacitor circuits, and filters. The fully-differential structure is extensively used in these applications because of its improved dynamic performance with respect to such aspects as signal-to-noise ratio(SNR) and total harmonic distortion(THD) when compared to its single-ended counterpart. In some of these applications, the fully-differential amplifier is required to have fast transient settling time without slew-rate limitations. Power consumption also must be taken into consideration because low power consumption can significantly reduce a battery's weight and size, and extend its life-time. A Class A amplifier is a difficult configuration in which to conciliate all these requirements, since its fixed bias current can limit its maximum output current. To simultaneously meet both slew-rate and power consumption requirements, several slew-rate enhancement(SRE) techniques have been proposed in the literature, but all of them are either incompatible with the low voltage operation or exhibit either degradation in linearity or increase in circuit complexity. This thesis presents a simple SRE technique, efficient in both power and area usage, improve the slew rate while overcoming the drawbacks of state-of-the-art SRE techniques.

In this work, several existing SRE techniques are discussed, and their advantages and disadvantages are identified. The proposed SRE technique is based on excess transient detection and feedback. A transient signal can be detected at the internal nodes of amplifier. Once the detected transient signal is found to be larger than a pre-defined turn-on value, the excess transient signal can be instantaneously amplified to turn on a dynamic current source and feed it back to the amplifier for current boosting. This pre-defined turn-on voltage results in a SRE circuit being solidly off during quiescent state. Small-signal performance and linearity of the original amplifier can be thus well preserved. Thanks to this excess transient feedback concept, the implementation is much simpler than that of previously reported methods, and the static

power overhead is also very small. Using the proposed SRE method, a fully-differential folded-cascode two-stage op-amp has been designed and fabricated using IBM 130nm process. This amplifier is designed to validate the proposed method of improving an amplifier's input-stage slew-rate. If the tail current doubles during slewing, the simulation result indicates that, at all corners, with temperature from 0 °C to 60 °C, the average slew-rate can be enhanced by a factor of 2.6 and the 1% settling time after a large input step is reduced by 30% compared to the vales without using SRE. Any further increment in the tail transient current can further increase the internal slew rate and eventually make it equal to the output-stage slew-rate.

It is well-known that self-stabilized circuits, such as current, voltage and frequency references, are vulnerable to a problem of multiple operating points; this is also known as the start-up problem. An op-amp can suffer from the same problem when performance enhancement feedback is being used. In particular, a slew rate enhancement circuit (SRE) can be used to provide performance enhancement in low-power high-speed op-amp design. For such circuits, a systematic method for detecting and removal of Trojan states is presented. Using a design example and simulation results, it is demonstrated that the proposed method can effectively remove a Trojan state in an op-amp without degrading the improved slew-rate.

CHAPTER 1. OVERVIEW

1.1 Introduction

The operational amplifier or "op-amp" is a fundamental building block in modern analog and mixed-signal systems. Its applications vary extensively from low-frequency subsystems, such as bandgap reference circuits and low-dropout regulator(LDO), to high-frequency subsystems such as analog-to-digital converters and phase-locked loops(PLL). Generally speaking, such amplifiers can find many uses in most mixed-signal subsystems, especially in ADCs/DACs, and the performance of these subsystems is heavily determined by amplifiers' performance. With the rapid pace of reducing CMOS technology transistor feature size, the supply voltage has been correspondingly scaled down to enforce device reliability and low power consumption on single VLSI cells. While digital circuitry can continuously gain benefits from feature size reduction in term of extremely speed improvement and shrinking cost, analog cells may on the other hand become more challenge. For mixed-signal design, both digital and analog circuitry are implemented on the same chip, implying that analog circuits must adapt to feature-size reduction evolution as well. As a result, it is not only required to design a small-area analog circuit using low supply voltage but, more importantly, to maintain high performance by following the rapid increase in digital circuitry operating speed.

However, this is very difficult to achieve in sub-micron technology, particularly for op-amp design, since the low supply voltage, short-channel effect and gate leakage can severely degrade many specs such as slew rate, dc gain, noise, SNR, swing range, linearity, etc. Such degradation has been demonstrated by measurement results from [1] and is shown in Figure 1.1. Because of short-channel effect, the intrinsic gain of the amplifier has been greatly reduced as shown in Figure 1.1(a), an adequate overall op-amp dc gain is hard to achieve. One solution is to cascade

more stages; this makes frequency compensation more difficult and also can significantly reduce the gain-bandwidth-product. Figure 1.1(b) shows that high-order harmonic components also increase in amplitude despite smaller signal as the technology scales down. Consequently, the THD significantly increases because the reduction of the supply voltage shrinks the signal swing and transistor's quiescent V_{DS}. Moreover, this shrinkage in signal swing range also can reduce the SNR, and might thus require more power consumption to maintain the same SNR level. The slew rate is also reduced due to the reduced voltage headroom.

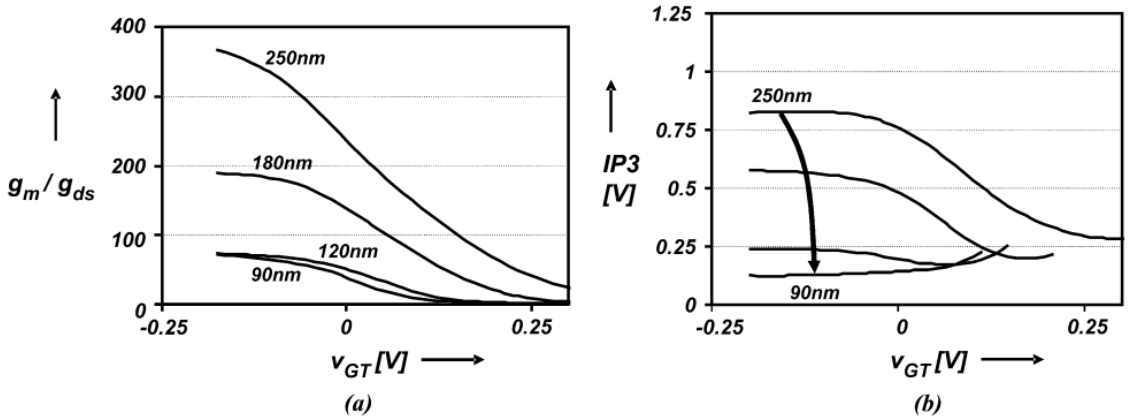

Figure 1.1 (a) intrinsic gain (b) output IP3 of transistor as a function of the gate-overdrive voltage with V_{DS} proportional to the nominal supply voltage (0.3V for 250nm) and L=1 μm for four technologies

The only way for analog circuitry to keep up with digital circuitry performance and supply voltage reduction is to apply performance enhancement techniques that can adapt low-voltage operations with high power efficiency and small die-area overhead. More specifically, for op-amps the existing performance enhancement circuitry can be divided into three categories: DC performance enhancement, small-signal transient performance enhancement and large-signal transient performance enhancement. A DC performance enhancement technique, as the name implies, is used to improve the amplifier's DC performance. It mainly includes DC gain, DC CMRR, and DC PSRR enhancement. DC gain enhancement technique is one of the most widely-published DC performance enhancement techniques in the literature. In particular, an efficient conductance cancellation method proposed in [2] can achieve at least a 26.4dB DC gain enhancement in 1.2V supply voltage design according to the reported measurement result.

Small-signal transient performance enhancement techniques are an extension of DC performance enhancement technique into the high frequency range. Last but not least, large-signal transient performance enhancement techniques, mainly referring to slew-rate enhancement techniques, may find wide use in high-precision and high-speed circuit design. The key purpose of improving amplifier's slew rate is to shorten the total settling time. In particular, for high-speed applications such as pipelined ADCs, the settling time strongly influences overall performance. For some other applications, the amplifier drives very large capacitive loads, thus requiring a large transient current at its output stage. Slew-rate enhancement techniques therefore become critical and many methods for achieving them have been reported in the literature over the past two decades.

1.2 Literature Review of State-of-the-Art SRE Technique

Many op-amp designs using different techniques to improve slew-rate have been reported in the literature [3]-[9]. Some have achieved better SRE efficiency than others but at the expense of more design complexity; some have less effect on the core amplifier while others can achieve faster detection with respect to slewing and may exhibit short delay times in turning on the SRE circuit. In the following subsections, two state-of-the-art slew enhancement techniques are reviewed, and their individual advantages and disadvantages are summarized.

1.2.1 Adaptive Biasing CMOS Amplifier

Adaptive biasing [3] is a very famous design technique for improving an amplifier's slew-rate. A single-stage OTA using an adaptive biasing scheme is shown in Figure 1.2. All the current mirrors have a ratio of 1 except the ratio of M17 to M18 and of M20 to M19; these two current mirrors both have a mirror ratio of A. When a positive differential signal V_{id} applied at the input, the drain current in M2, designated as I_2, becomes much larger than that in M1, designated as I_1. The absolute value of current difference $|I_1 - I_2|$ is sensed by the current subtraction circuit formed by M16-M21 and amplified by a factor of A to add to the tail current of the OTA. If it is assumed that input transistor M1 and M2 are both operating in the weak inversion region and that $V_{id} = V_{in+} - V_{in-} > 0, I_2 - I_1 > 0$, by applying Kirchhoff's current

law at node X to produce Equation(1.1) and the current relationship between I_1 and I_2 to produce Equation(1.2), the current expressions of M1 and M2 can be derived as Equation (1.3) and (1.4)

$$I_1 + I_2 = A|I_1 + I_2| + I_p \tag{1.1}$$

$$I_1 = I_2 e^{V_{id}/nV_T} \tag{1.2}$$

$$I_1 = \frac{I_p e^{V_{id}/nV_T}}{(A+1) - (A-1)e^{V_{id}/nV_T}} \tag{1.3}$$

$$I_2 = \frac{I_p}{(A+1) - (A-1)e^{V_{id}/nV_T}} \tag{1.4}$$

The current follows into the load is expressed as

$$I_1 = I_1 - I_2 = \frac{I_p(e^{V_{id}/nV_T} - 1)}{(A+1) - (A-1)e^{V_{id}/nV_T}} = \frac{I_p}{1-A}[1 - \frac{2}{(1+A) + (1-A)e^{V_{id}/nV_T}}] \tag{1.5}$$

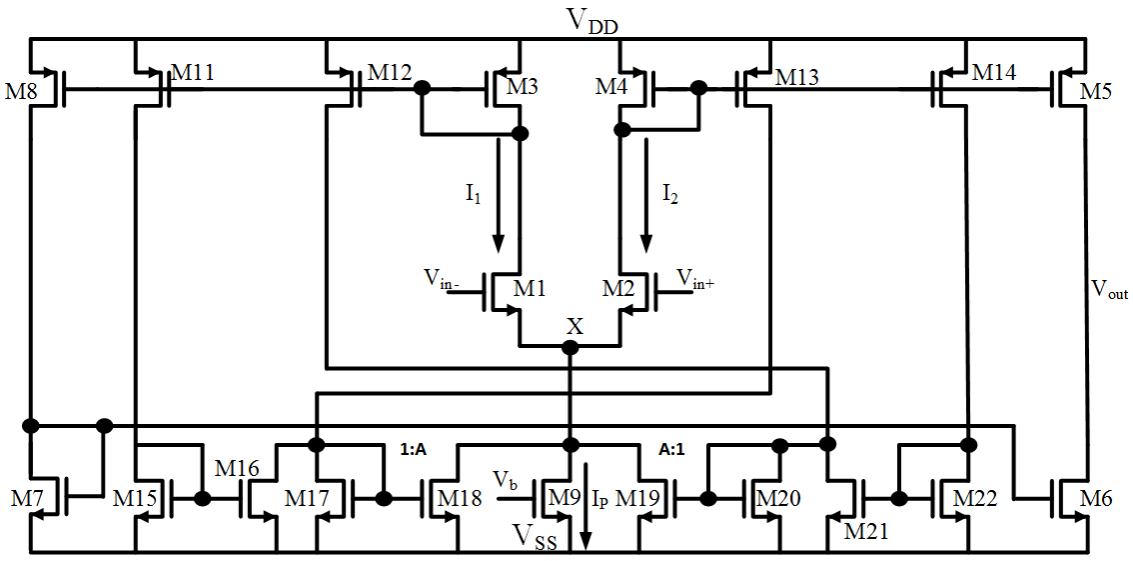

Figure 1.2 Adaptive bias OTA from [3]

During amplifier slewing, a large differential signal is applied at the input and thus $V_{id} >> nV_T$, so the maximum current charging the load, derived as

$$I_{pk} = I_{out|V_{id}>>nV_T} = \begin{cases} \frac{I_p}{1-A} & \text{if } 0 \leq A < 1 \\ unpredicted & \text{if } A \geq 1\ . \end{cases} \tag{1.6}$$

The Equation (1.6) implies that when $A = 1$ the peak current in the load can be very large but never infinite since the input pair will leave the weak inversion region and Equation (1.2)

will be invalid. For example, if A is set to 0.9, then the slew rate can be improved by factor of 10 compared to the value without adaptive biasing. For small-signal operation, Equation (1.2) always holds when biasing an input pair in weak inversion (true in most cases), and the transconductance of input pair can be derived as Equation (1.7)

$$g_{m1,2} \approx \frac{\partial I_{out}}{\partial V_(id)} = \frac{2I_p}{nV_T[(1+A)^2(1-\frac{V_{id}}{nV_T}) + (1-A)^2(1-\frac{V_{id}}{nV_T}) + 2(1-A^2)]} \tag{1.7}$$

Equation (1.7) shows that, with variation of the input differential signal, $g_{m1,2}$ always stays constant when $A = 0$, but will vary as long as $A \neq 0$, so one obvious drawback of adaptive-bias-based slew-rate enhancement technique is degradation in linearity of the original core amplifier. This is because the adaptive bias circuit cannot distinguish between small-signal and large-signal operation. A more intuitive understanding of this result is that the adaptive biasing scheme forms a positive feedback loop for differential signals and the input transconductance hence becomes larger with an increase in input differential signal. In addition, since the optimal value of A is determined by current mirror M17, M18 and M19, M20 matching performance, this SRE technique will not be robust with respect to PVT variation.

1.2.2 Slew-Rate and Gain Enhancement in Two-Stage Operational Amplifiers

The SRE method proposed in [4] enhances the slew rate by implementing a push-pull structure to adaptively increase the tail current and output stage transient current during slewing. The complete circuit schematic shown in Figure 1.3 illustrates application of this method to a two-stage fully-differential amplifier. The circuit in Figure 1.3(a) is used to detect slewing of the core amplifier in Figure 1.3(b). The four output voltages V_A, V_B, V_C and V_D in Figure 1.3(a) are used to dynamically bias the PMOS current sources M3 and M4, tail currents Ma16 and Ma17 and NMOS current sources Ma9 and Ma18. The simulation result of [4] shows that both positive and negative slew rate can be enhanced by more than a factor of 4. However, the drawbacks of this slew rate method are also obvious. First, the slewing is sensed at the input of the amplifier, that is very sensitive to any transistor mismatch. Second, the circuit has a positive feedback loop for differential signal path; this can increase the distortion and degrade linearity as in the adaptive biasing method. The positive feedback loop for common-

mode signal also can induce the multiple operating point issue for this circuit. Third, even-order harmonics cannot be suppressed as in conventional fully-differential amplifiers since the common source node of an input pair is not virtual ground. Finally, the silicon area overhead of this SRE method is significantly large.

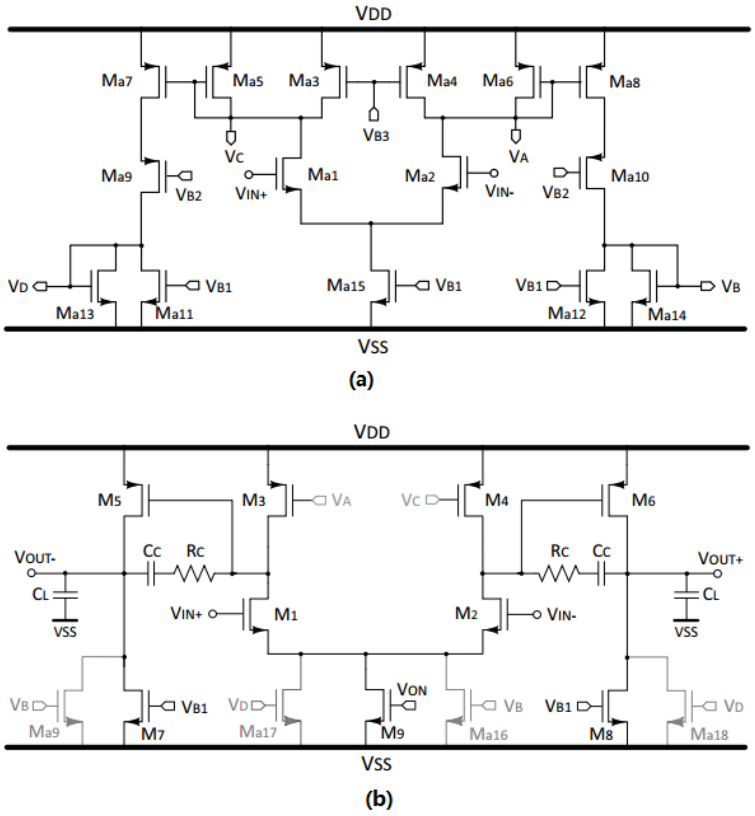

Figure 1.3 (a)main circuit (b)SRE monitor circuit from [4]

1.3 Research Contribution and Thesis Organization

In this thesis, a novel method on slew rate enhancement based on excess transient detection and feedback is presented. In Chapter 2, the basic concept of SRE technique via excess transient feedback is first described and a circuit implementation is then provided along with a detailed quantitative analysis. In chapter 3, the design of a folded-cascode fully differential two-stage amplifier implemented in IBM 130nm process with the proposed slew rate enhancement technique is shown along with simulation results. Large-signal transient analysis is per-

formed on the proposed op-amp. To accommodate the folded-cascode structure and achieve symmetry of the improved slew rate, a cascode-stage current-boosting method is proposed. Chapter 4 illustrates that the SRE circuit can induce undesired operating points (also known as"Trojan states") issue into the op-amp. For such a circuit, a systematic method for detecting and removing Trojan State is presented. Using a design example and simulation results, it is demonstrated that the proposed method can effectively remove Trojan states in the op-amp. Chapter 5 presents conclusion from the work presented in this thesis along with the plan for future work on this topic.

CHAPTER 2. SRE VIA EXCESS TRANSIENT FEEDBACK

2.1 Introduction

Slew rate is the key large-signal specification of an op-amp used to measure the maximum achievable voltage change rate at each output node. As the input signal amplitude of the conventional single-ended folded-cascode amplifier shown in Figure 2.1 increases, non-linearity will appear at the op-amp output due to the inadequate slew rate. For the op-amp in Figure

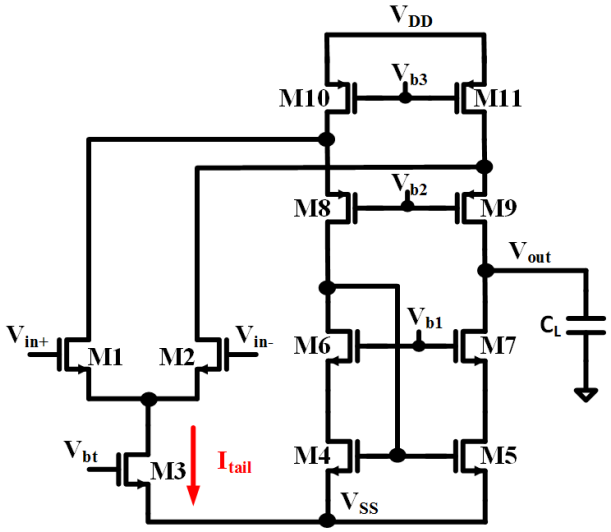

Figure 2.1 Conventional single-ended folded-cascode op-amp

2.1, the gain-bandwidth-product and slew rate are given by

$$GBW = \frac{g_{m1}}{C_L} \tag{2.1}$$

$$SR = \frac{I_{tail}}{C_L} \tag{2.2}$$

By taking the ration of SR and GBW, result is given by

$$\frac{SR}{GBW} = \frac{I_{tail}/C_L}{g_m/C_L} = \frac{I_{tail}}{C_L} = \frac{2I_1}{C_L} \tag{2.3}$$

For the case of input transistor pair works in strong inversion region(roughly $V_{OD1} > 0.2V$), Equation (2.3) is simplified as

$$\frac{SR}{GBW} = \frac{2I_1}{C_L} = V_{OD1} \geq 0.2V \tag{2.4}$$

For the case of input pair works in weak inversion region (roughly $V_OD1 < 80mV$), Equation (2.4) is simplified as

$$\frac{SR}{GBW} = \frac{2I_1}{C_L} = 2nV_T \approx 0.1V \text{at room temperature} \tag{2.5}$$

If the op-amp is used to amplify a sinusoidal signal and the output differential signal can be expressed as

$$V_{out}(t) = \frac{V_{pp}}{2} sin(\omega t) \tag{2.6}$$

where V_{pp} is the output signal swing and ω is fundamental frequency. The output signal slop is expressed as

$$\frac{dV_{out}}{dt} = \frac{V_{pp}GBW}{2} cos(\omega t) \tag{2.7}$$

Assume $V_{pp} = V_{DD}/2$ and $V_{DD} = 1.2V$. The maximum slop of output signal occurs when $\omega = GBW$ and $cos(\omega t) = 1$, which is given by

$$[\frac{dV_{out}}{dt}]_{max} = \frac{V_{pp}GBW}{2} \tag{2.8}$$

In order to avoid slew rate induced distortion, it requires to satisfy

$$SR \geq [\frac{dV_{out}}{dt}]_{max} = \frac{V_{DD}GBW}{4} \tag{2.9}$$

By re-ranging (2.9), yields

$$\frac{SR}{GBW} \geq \frac{V_{pp}GBW}{2} = \frac{V_{DD}}{4} = 0.3V \tag{2.10}$$

According to Equations (2.3), (2.4) and (2.10), an input transistor pair has to work in strong inversion region to avoid slew-rate induced distortion for a given output swing range. This large gate-overdrive voltage significantly decreases g_m efficiency, defined as g_m/I_D. In other words, for a given current budget and capacitive load, a lower input transconductance is obtained, resulting in a lower GBW and higher input-referred offset and noise.

The conventional constant tail current source op-amp therefore imposes an inadequate slew rate, and thus design tradeoffs between GBW, slew rate, offset, noise, and harmonic distortion may be required. To relax those design tradeoffs, many slew-rate enhancement techniques have previously been reported. In this chapter, a novel slew-rate enhancement technique based on excess transient detection and feedback is presented. This technique has several advantages over previously-reported SRE methods. First, the SRE circuit has a well-defined turn-on voltage. For small-signal operation, the sensed transient voltage is less than this pre-defined turn-on voltage and hence the SRE stays off and therefore has no impact on the core amplifier's small-signal performance and linearity. Second, the boosted transient current can be quantitatively defined so that the maximum achievable slew rate is known. Third, the proposed method is robust to input common-mode voltage and PVT because slewing is detected at amplifier's internal nodes rather than at input or output nodes. Finally, the area and power consumption overhead are both very small.

2.2 The Concept of Excess Transient Feedback

The slew-rate enhancement method using excess transient feedback was initially introduced in [6]. The conceptual block diagram for the excess-transient-feedback-based SRE scheme is shown in Figure 2.2. The transient signal x_s is sensed at the output stage, which could be either a single-ended or differential voltage or current signal. Then the generated control signal x_{fb} is used to turn on/off the dynamic current source. x_{fb} is a non-linear function of x_s and they have the relationship as shown in (2.11), where α is a non-constant gain factor and x_{th} is the pre-defined turn-on voltage of the SRE circuit.

$$f(x_s) = \begin{cases} \alpha(x_s - x_{th}) & \text{if } |x_s| > x_{th} \\ 0 & \text{if } |x_s| \leq x_{th} \ . \end{cases} \tag{2.11}$$

When the amplifier is at its DC operating point or in small-signal operation, i.e., when $|x_s| \leq x_{th}$, the generated control signal x_{fb} is always zero and the dynamic current source is turned off, so the amplifier will preserve its original small-signal performance. However, when the output stage of the amplifier begins to slew, that is when $|x_s| > x_{th}$, the control signal x_{fb},

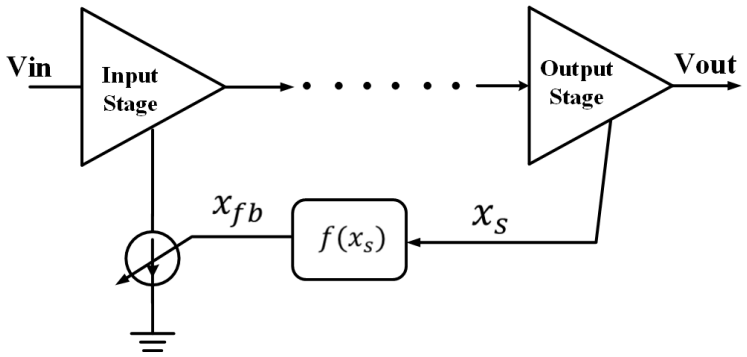

Figure 2.2 Conceptual block diagram of excess transient feedback based SRE scheme

a product of the non-constant gain factor α and excess transient signal, $x_s - x_{th}$, will turn on the dynamic current source to boost the slew rate. To ensure full turn-off of the SRE circuit during small-signal operation and fast turn-on during slewing, the value of x_{th} and α must be properly chosen.

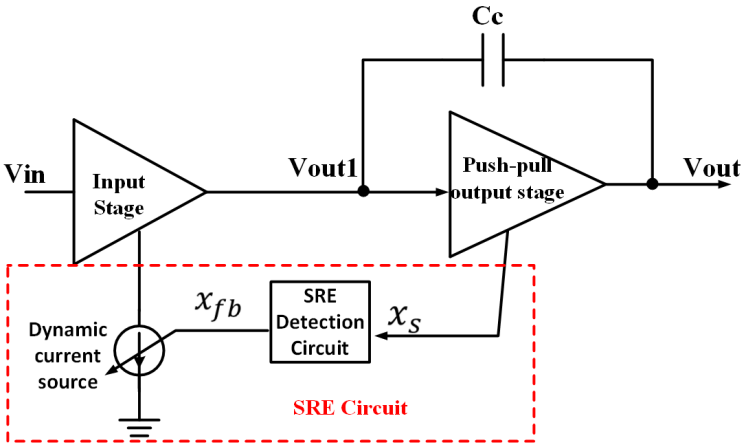

Figure 2.3 Conceptual block diagram of two-stage push-pull op-amp with proposed SRE scheme

In particular, for a two-stage op-amp with a push-pull output stage (as shown in Figure 2.3), the dominant slew-rate limitation is the charging/discharging rate of the compensation capacitor C_c (also called internal slew-rate). Since the charging/discharging rate of C_c is determined by the tail current of the op-amp (also the C_c value), the proposed slew-rate enhancement circuit can be applied to sense the slewing at the push-pull output stage and turn on extra dynamic current to boost the tail current at large-signal transient operation.

2.3 Circuit Implementation

The circuit implement of the proposed SRE circuit is shown in Figure 2.4. M37 and M38 are dynamic current sources and their drains are connected to the common-source node of the core amplifier input pair. M35 and M36 are two switches that can dynamically control the dynamic current source. M37 and M38 are normally off for preserving small-signal performance and the linearity of the core amplifier. Once the amplifier begins to slew, one of the switches M35 and M36 will be heavily tuned on so that additional current can be provided to the tail for boosting the core amplifier's slew-rate.

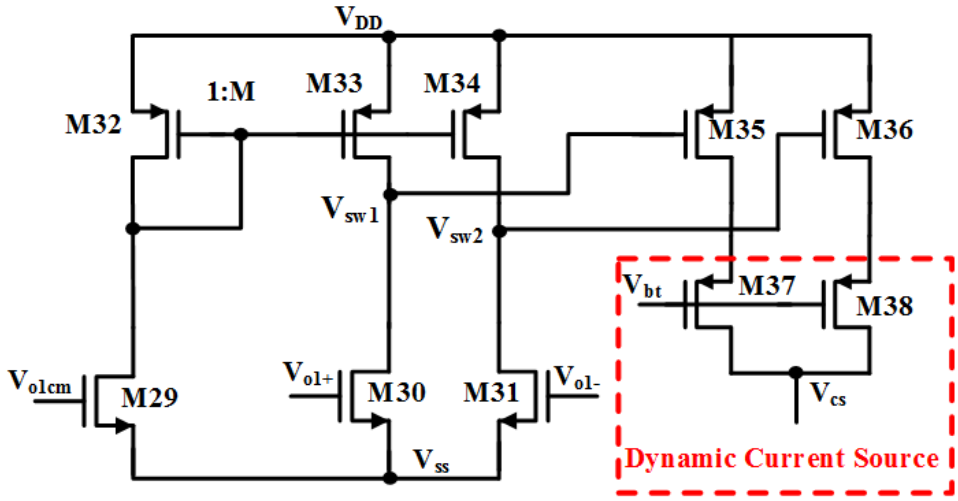

Figure 2.4 Circuit implementation of SRE circuit

In the proposed slew-rate-enhancement circuit shown in Figure 2.4, M29-M34 comprise the SRE detection circuit part in the conceptual block diagram shown in Figure 2.3. The gates of M30 and M31 are connected to the amplifier's internal nodes V_{o1+} and V_{o1-}, respectively, and used to detect the slewing. V_{o1+} and V_{o1-} have the same common-mode voltage V_{o1cm} but opposite differential voltages. The gate of M29 is biased with the common-mode voltage V_{o1cm}. The transistors M29, M30, and M31 have the same aspect ratio, while both M33 and M34 have a size ratio M with respect to M32. At quiescent point, to make sure M30 and M31 are operating in saturation while M33 and M34 are operating in the triode region, a value of $M > 1$ is chosen. The reason for having M30 and M31 in saturation and M33 and M34 in triode is to

turn off the dynamic current source M37 and M38 and make sure that the SRE circuit has no impact on the core amplifier. Due to the symmetry of the SRE circuit, the following analysis will only be applied to the V_{o1+} side, and the same result can also be applied to V_{o1-} side.

At quiescent point, M29, M30 and M31 have the same gate-source overdrive voltage V_{OD29} and these three transistors are all in saturation. M33 is operating in triode region. The drain current of M30 is equal to the drain current of M33, which gives

$$\beta_{33}(V_{od33} - \frac{1}{2}V_{ds33})V_{ds33} = \frac{1}{2}\beta_{32}V_{od33}^2 \tag{2.12}$$

where $\beta_{33} = \mu_p C_{ox} W_{33}/L_{33}$ and $\beta_{32} = \mu_p C_{ox} W_{32}/L_{32}$
Since $\frac{W_{33}/L_{33}}{W_{32}/L_{32}} = M$, then the relation between β_{33} and β_{32} is as

$$\frac{\beta_{33}}{\beta_{32}} = M \tag{2.13}$$

According (2.12) and (2.13), the drain-source voltage of M33 is written as

$$V_{ds33} = (1 - \sqrt{1 - \frac{1}{M}})V_{od33} \tag{2.14}$$

To ensure dynamic current source M37 is off, $V_{ds33} < V_{th35}$ requires to be satisfied. V_{th35} is the threshold voltage of switch transistor M35. By applying Equation (2.14), this condition can be written in terms of M32 gate-source overdrive voltage and current mirror ratio M as (2.15)

$$(1 - \sqrt{1 - \frac{1}{M}})V_{od33} < V_{th35} \tag{2.15}$$

Under the conditions of (2.15), the threshold voltage V_{th35} is known once the switch size M35 has been determined and the gate-source overdrive voltage of M33 defined by the designer. Since M32 and M33 comprises a current mirror, the gate-source overdrive voltage of M33 is often set to lie in the range of 250mV to 350mV, and as a result, the minimum value of the current mirror ratio M can be determined.

When a differential signal V_{id} is applied on the input of the core amplifier, the sensed complementary signals V_{o1+} and V_{o1-} changing in the opposite direction can be described as $V_{o1+} = V_{o1cm} + \Delta V$ and $V_{o1-} = V_{o1cm} - \Delta V$ respectively. Obviously, $|\Delta V|$ increases as V_{id} increases. When $|\Delta V| < V_{od29}$, both M30 and M31 remain turned on. When $|\Delta V| > V_{od29}$,

either M30 or M31 turns off. When $|\Delta V|$ reaches the same value as the turn-on voltage ΔV_{on}, either M33 or M34 begins to enter the saturation region and M30 or M31 is about to leave the saturation region. Any further small increment on ΔV will then immediately push M30 or M31 into the triode region and simultaneously turn on either switch M35 or M36 to enable dynamic current source. The turn-on voltage of SRE circuit can therefore be defined as the $|\Delta V|$ that can result in both M30 and M33 or both M31 and M34 operating in saturation. By applying a KCL equation at the drain of M33 as in Equation (2.16), the turn-on voltage $|\Delta V_{on}|$ can be expressed as shown in Equation (2.17).

$$\frac{1}{2}\beta_{30}(V_{od29} + \Delta V_{on})^2 = \frac{1}{2}M\beta_{30}V_{od29}^2 \tag{2.16}$$

$$\Delta V_{on} = (\sqrt{M} - 1)V_{od29} \tag{2.17}$$

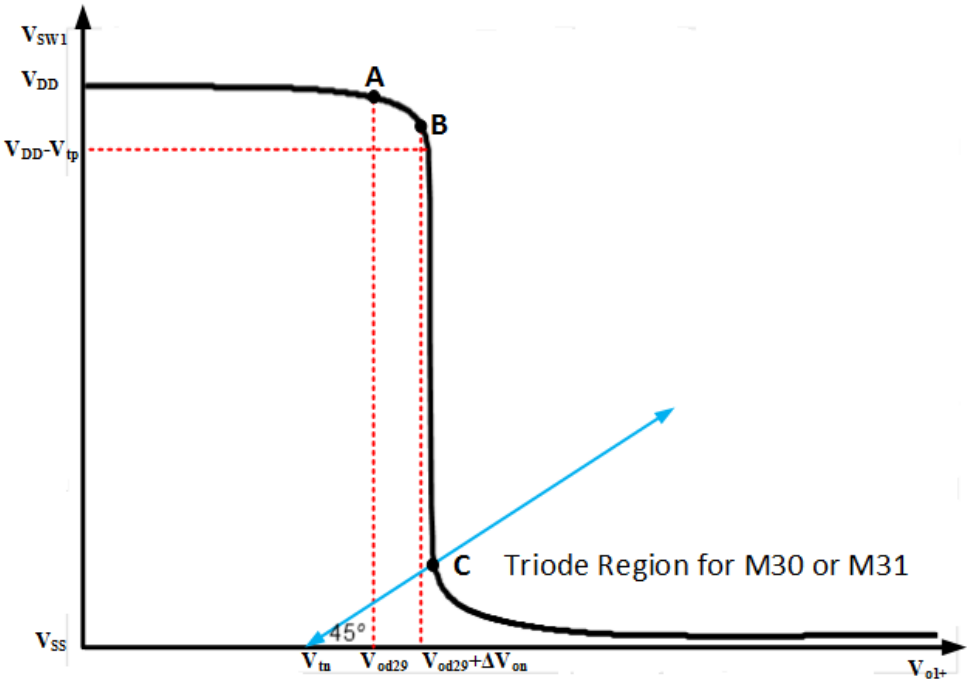

Figure 2.5 Sensed voltage V_{o1+} vs switching signal V_{sw1}

For large-signal operation, $|\Delta V|$ is large, resulting in M30 or M31 operating in the deep triode region and V_{sw1} and V_{sw2} can be as low as V_{ss}. The source of M37 and M38 can therefore be as high as V_{DD} and fully turn on the dynamic current source M37 and M38. One thing

must be mentioned is that, once the dynamic current source M37 and M38 are fully turned on, the amount of dynamic current adding into the tail is determined by the size ratio of M37 and M38 with respect to the amplifier's tail-current-source transistor.

Figure 2.5 shows the plot of sensed voltage V_{o1+} vs switching signal V_{sw1}. The region between B and C on the plot corresponds to a range where both M30 and M33 or both M31 and M34 are in saturation. The steeper the curve in this region, the faster the dynamic current source is turned on. This means that large gain from node V_{o1+} to V_{sw1}, as the coefficient α in (2.11), is required, which can be achieved by generating a large g_m for M30 and M31 and high resistance at the drain of M33 or M34.

CHAPTER 3. DESIGN OF TWO-STAGE FULLY-DIFFERENTIAL FOLDED-CASCODE OP-AMP

3.1 Introduction

It is well-known that a fully differential operational amplifier exhibits improved dynamic performance over its single-ended counterpart. One advantage of a fully differential amplifier is that it reduces even-order harmonics. Assuming a well-matched fully differential amplifier and expanding the transfer function of the circuit into a power series form as shown below,

$$V_{o1+} = k_1(V_{i+} - Vi-) + k_2(V_{i+} - V_{i-})^2 + k_3(V_{i+} - V_{i-})^3 + ... \tag{3.1}$$

$$V_{o1-} = k_1[-(V_{i+} - Vi-)] + k_2[-(V_{i+} - V_{i-})]^2 + k_3[-(V_{i+} - V_{i-})]^3 + ... \tag{3.2}$$

$$V_{od} = V_{o+} - V_{o-} = 2k_1(V_{i+} - V_{i-}) + 2k_3(V_{i+} - V_{i-})^3 + ... \tag{3.3}$$

where k_1, k_2 and k_3 are constant.

As shown in (3.2)-(3.3), the odd-order harmonic terms retain their alternate polarities while the even-order terms are always positive, so when the differential is taken, the even-order term will be canceled out. Another advantage of this configuration is that it increases the output swing range. Because of the change in phase between the differential outputs, the output voltage swing increases by factor of two over a single-ended output with the same voltage swing. The plot from [10] shows this advantage intuitively in Figure 3.1. In addition, the fully-differential amplifier can exhibit increased noise immunity. Since the circuit is fully symmetric, any common-mode noise will appear equally at both output terminals and is canceled when making differential. Since the output swing range is doubled, the signal-to-noise ratio (SNR) is also twice as large.

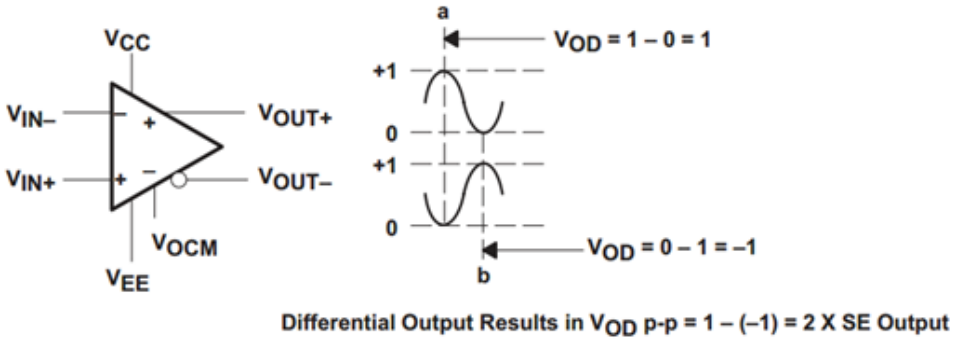

Figure 3.1 Differential output voltage swing [10]

However, one limitation of the fully differential amplifier is extra common-mode feedback (CMFB) circuitry is required to fix the common-mode voltage at high impedance nodes that are not stabilized by negative differential feedback. Especially, for a rail-to-rail output fully differential amplifier, two CMFB circuits are often required to stabilize both input-stage and output-stage common-mode voltage. Without a CMFB circuit, common-mode voltage drifting can cause differential signals to move into the triode region and clipping can cause non-linearity in the differential signal as illustrated in Figure 3.2. With the CMFB circuit, the output

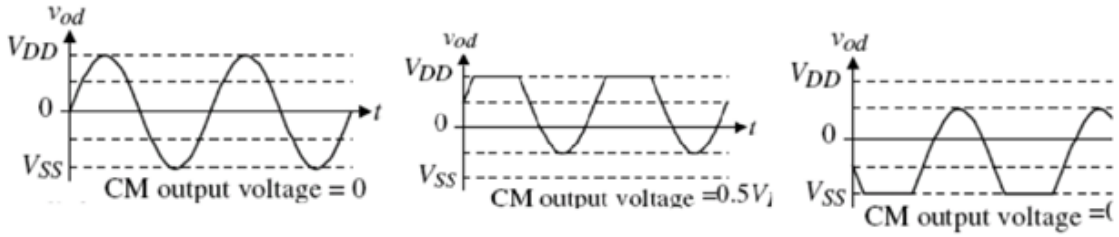

Figure 3.2 Effect of output common-mode voltage drifting [11]

common-mode voltage is held at the middle of the output swing range. This is achieved by sensing the output common-mode voltage and comparing it to the desired output common-mode voltage. By applying negative feedback, if the output common-mode voltage is lower than the desired common-mode voltage, the CMFB circuit operates to increase the output common-mode voltage. Conversely, it will lower the output common-mode voltage under opposite condition.

In this chapter, the detailed design of a two-stage fully differential folded-cascode op-amp is presented. Using the proposed SRE scheme described in the previous chapter, its slew-rate can be improved by factor of 2.61 over all process corners and temperatures ranging from 0 °C to 60 °C. In addition, to make the improved slew-rate still symmetrical, a cascode-stage current-boosting method is proposed and implemented in the designed op-amp. The simulation results show that the enhanced slew-rate can be guaranteed to be symmetric over all the process corners and temperature from 0 °C to 60 °C. The power and area overhead is only 3.6% and 13.3% respectively.

3.2 g_m/I_d Based Op-amp Design

3.2.1 Why g_m/I_d Is Important

g_m/I_d design methodology is a widely used method in op-amp design. As shown in Figure 3.3, the g_m/I_d value with respect to drain current density for different channel lengths, we can observe that g_m/I_d value keeps the same for a given transistor drain current density regardless of transistor's channel length.

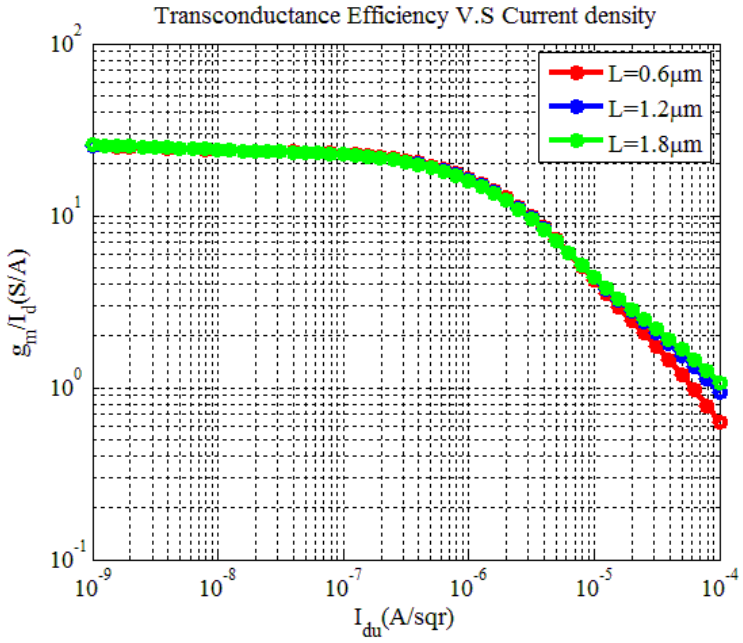

Figure 3.3 Transconductance efficiency v.s current density

Moreover, the transistor operating region can be easily defined from the g_m/I_d plot. For $I_{du} < 500nA/sqr$, g_m/I_d is nearly constant with current density variation; this corresponds to the weak region. Transistors biased in this region can achieve highest transconductance efficiency in a certain technology. For low-power design, transistors are often expected operated in this region. When the current density $I_{du} > 5uA/sqr$, the g_m/I_d curve linearly changes with the drain current density. This region corresponds to a strong inversion region, in which a square-law model can well describe transistor operational behavior. The boundary between the weak region and the strong inversion region on the plot is the moderate inversion region. Operating transistors in moderate inversion is optimal when we equally value speed and power efficiency in the design. This is because transistors achieve maximum transconductance efficiency with low speed in the weak inversion region while transistors gain faster speed but with very low transconductance efficiency in strong inversion (as in Figure 3.4(b)). As shown in Figure 3.4(b), in the moderate inversion region transistors can gain maximum value of the product of speed and transconductance efficiency. Unfortunately, there is not a good model equation to describe transistors operating in the moderate inversion region.

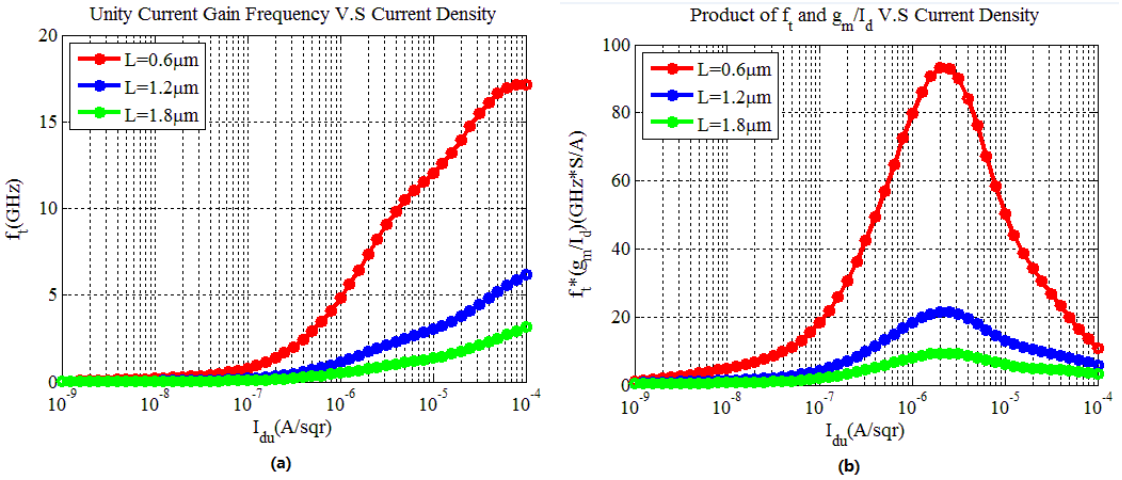

Figure 3.4 (a)unity current gain frequency v.s current density (b) product of f_t and g_m/I_d v.s current density

Summary, the g_m/I_d design method is important from the following perspectives. First, the g_m/I_d curve is generated directly from SPICE simulation and is therefore linked to the actual measurement data. This makes the design a better match with the final fabricated one. Second,

the g_m/I_d value does not depend on any model equation; this has the benefit of avoiding certain design uncertainties. Third, g_m/I_d curves have fixed shapes regardless of transistor channel length. In other words, for a certain current density the g_m/I_d value has very little variation with respect to the transistor channel length. Last, but not least, the g_m/I_d value can relate one design specification to another. For example, the GBW specification of a two-stage op-amp can be related to its SR specification by $GBW = g_m/C_c = g_m/(I_d/2) \times (I_d/C_c) = 2 \times (g_m/I_d) \times SR$. Because of these advantages of g_m/I_d design methodology, the two-stage fully differential folded-cascode op-amp presented in this chapter has been designed based on the generated g_m/I_d curve for IBM 130nm technology.

3.2.2 Op-amp Structure and Sizing Strategy Based on g_m/I_d Curve

The structure of the proposed two-stage op-amp is given in Figure 3.5. It has a folded-cascode input stage followed by a class AB output stage. The input pair is folded into a cascode-stage at nodes V_{f1} and V_{f2}. In the first stage, both the PMOS side and NMOS side are cascoded for the purpose of boosting the output impedance. The reason that the NMOS side has one more cascode transistor than the PMOS side is to ensure that the impedance looking upward at nodes V_{x1} and V_{x2} is of the magnitude $1/g_m$ and is much smaller than the impedance looking downward at those nodes so that all the compensation current can follow towards the first stage output nodes V_{o1+} and V_{o1-} to achieve high compensation efficiency.

For the output stage, since a fully-differential first stage is used, the most straightforward method to achieve a Class AB output stage is to use one first-stage output such as V_{o1-} to drive transistor M17 directly, and the other output V_{o1+} has to be inverted for driving M19 [12]. Since the first stage is a fully differential structure, a CMFB circuit is required. This circuit sets the common-mode voltage of the first stage that is used at the same time to control V_{GS} of M16-M17 and M22-M23, thus also controlling the quiescent current in the output stage. Also, due to the differential structure of the second stage, another CMFB circuit consisting of M15 and M21 is required to control the output common-mode voltage of the second stage.

The sizing strategy for each transistor is mainly based on the setting of their g_m/I_d values. In general, for those transistors used for current sources/sinks, g_m/I_d is set to be relatively low

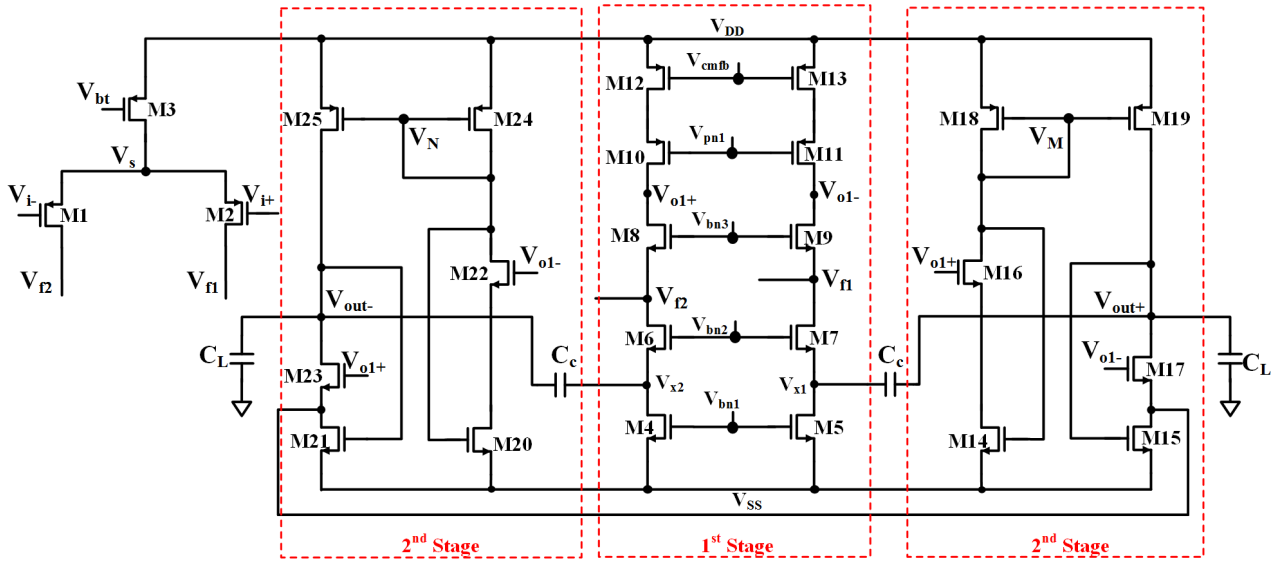

Figure 3.5 Structure of proposed two-stage op-amp

so as to achieve large gate-source overdrive voltage to reduce the current mismatch between each current source. However, for the first-stage input pair and second-stage input transistors, a high g_m/I_d value is required to achieve optimal power efficiency and speed, and lower input-referred offset. The chosen g_m/I_d value of transistors shown in Figure 3.5 are summarized in the following Table 3.1.

3.3 Slew-Rate Enhancement Circuit

In this section, large-signal transient analysis is first performed on the designed two-stage op-amp, as shown Figure 3.5. From this analysis, the dominant source for slew-rate limitation can be found. Then the proposed SRE scheme described in Chapter 2 is utilized for improving the op-amp's slew-rate. In addition, for the purpose of ensuring the symmetry of enhanced slew-rate on charging and discharging sides, a cascode-stage current-boosting method is also proposed and implemented. Simulation results are provided to show effectiveness in improving slew-rate, and comparison between the design with the proposed SRE method and without this method is also shown in this section.

Table 3.1 Summary of transistor g_m/I_d values

Transistor	$g_m/I_d(S/A)$	**Function**
M1, M2	18.95	input pair
M3, M12, M13	12	PMOS side current source
M10, M11	20	PMOS side cascode transistor
M18, M19, M24, M25	14	Second stage PMOS current mirror
M8, M9	29.1	NMOS cascode transistor
M6, M7	24	NMOS cascode transistor, voltage buffer
M4, M5	19	NMOS side current source
M16, M17, M22, M23	15	second stage input transistor

3.3.1 Large-Signal Transient Analysis

When a large differential signal V_{id} is applied at the op-amp input, two complementary differential transient currents are generated in the differential pair. When the $|V_{id}|$ is sufficiently large to fully turn off one side of the differential pair, the circuit is in slewing. In this case, all the tail current can only flow through one side of the input differential pair.

Figure 3.6 shows analysis of the transient current in the op-amp during slewing. $(1/2)I_{ss}$ transient current flows in opposite directions in M1 and M2. That is, $(1/2)I_{ss}$ transient current is flowing into node V_{f2} while $(1/2)I_{ss}$ transient current is flowing out of node V_{f1}. Since the currents in the PMOS current source transistors M12 and M13, and NMOS current source transistors M4 and M5 are constant during slewing, the $(1/2)I_{ss}$ transient current flowing into node V_{f2} is all used to charge compensation capacitor C_c on the left-side and the $(1/2)I_{ss}$ transient current flowing out of node V_{f1} results from the discharging of compensation capacitor C_c on the right-side. The slew-rate at V_{o1+} can be expressed as

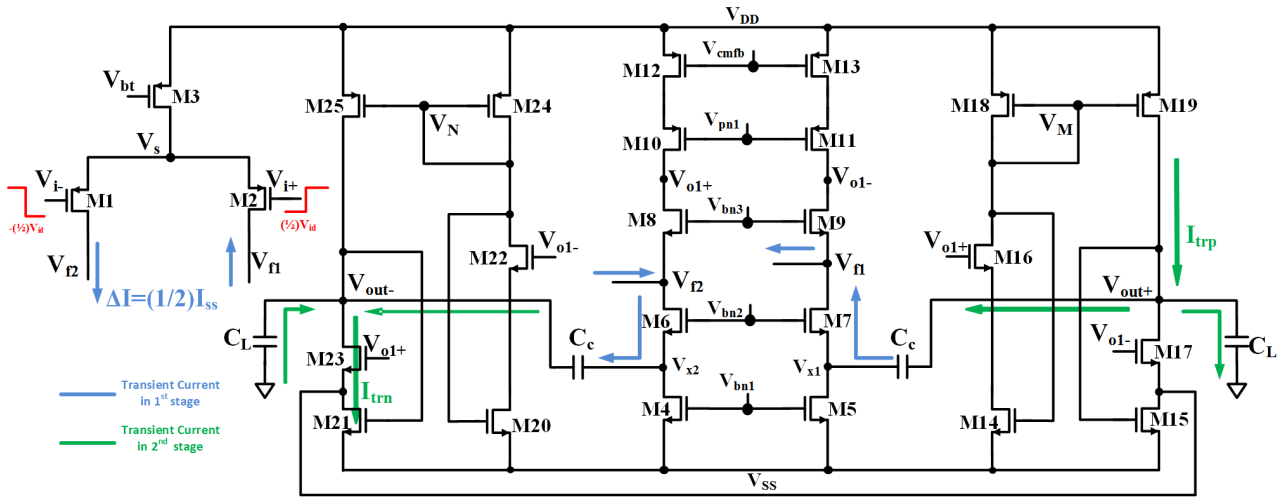

Figure 3.6 Transient current in op-amp during slewing without SRE

$$SR_+ = \frac{I_{ss}/2}{C_c} \tag{3.4}$$

The slew-rate at V_{o1-} can expressed as

$$SR_- = \frac{-I_{ss}/2}{C_c} \tag{3.5}$$

The differential slew-rate for the first stage is expressed as

$$SR = SR_+ - SR_- = \frac{I_{ss}}{C_c} \tag{3.6}$$

Equation (3.4) and (3.5) indicate that, by the nature of the differential structure, the slew-rate in the first stage is symmetric.

For the output stage, on one-side the NMOS is heavily over-driven and the PMOS is fully turned off, while on the other side the PMOS is heavily over-driven and NMOS is fully turned off. For the case shown in Figure 3.6, the gate of transistor M17 is turned off since V_{o1-} is swinging downwards near V_{ss} and V_{o1+} is driving the intermediate stage transistor M16 to heavily turn on transistor M19. Consequently, the transient current I_{trp} drawn from M19 will

charge C_L and C_c simultaneously. On the other side, M23 is directly over-driven by first stage output V_{o1+} to generate large transient current I_{trn}, while M25 is fully turned off. Consequently, this large transient current I_{trn} is discharging both C_L and C_c. The slew rate at two output nodes can be expressed as

$$SR_o+ = \frac{I_{trp}}{C_c + C_L} \tag{3.7}$$

$$SR_o- = \frac{-I_{strn}}{C_c + C_L} \tag{3.8}$$

Equation (3.7) and (3.8) indicate that the condition of achievement of output stage slew-rate symmetry occurs when $I_{trp} = I_{trn}$. However, since the output stage is in class AB operation, a large dynamic current can be generated to either charge or discharge load capacitors. For example, according to the square law model, when the first-stage output swings up to 3 times the gate-source overdrive voltage of the second-stage input transistor, the generated transient current in the output stage is about 9 times its quiescent current. As a result, the overall slew-rate of the two-stage op-amp with a class AB output stage is limited by the first-stage slew-rate, as shown in Equations (3.4)-(3.6). By using indirect compensation, the compensation capacitor values can be reduced but slew-rate can only be slightly improved. A more effective way to improve the first-stage slew-rate is to add transient current at the tail for increasing the I_{ss} value during slewing.

3.3.2 Tail-Current Boosting

The two-stage op-amp with a tail-current boosting method is shown in Figure 3.7. The SRE detection scheme consisting of transistor M29-M34 is the same as that described in Chapter 2. Transistor M35 and M36 both work as switches to dynamically control the current sources M37 and M38. To quantitatively control the amount of dynamic current generated by the SRE circuit, transistors M37 and M38 are set to have a size ratio of N with respect to quiescent current source M3. Also, for the purpose of achieving good matching for the current among

transistors M3, M37, and M38, an additional switch transistor M39 is added onto the drain side of quiescent current source M3 with its gate connected to ground.

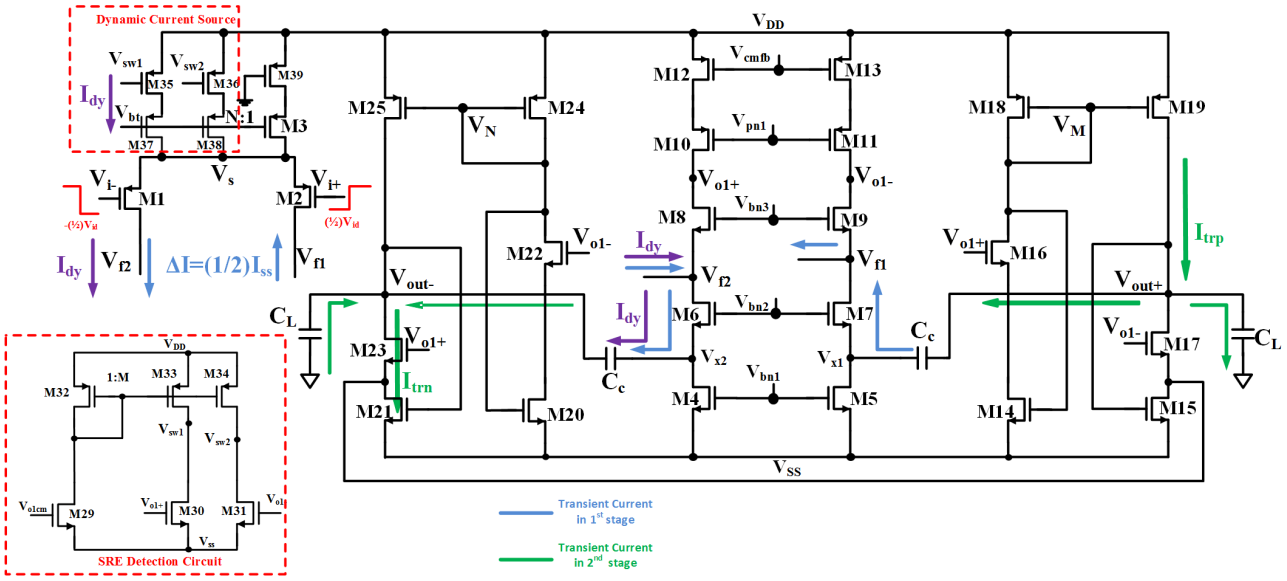

Figure 3.7 Two-stage op-amp with tail current boosting

In this design, value of N is set to 1 so that theoretically the total tail current is boosted by factor of 2. As illustrated in Figure 3.7, the boosted dynamic current I_{dy} is all flowing into node V_{f2} for charging the C_c on the left-side. The boosted slew-rate at V_{o1+} is expressed as

$$SR_+ = \frac{3I_{ss}}{2C_c} \tag{3.9}$$

The slew-rate at V_{o1-} is unchanged as (3.5) because no extra discharging current is provided for the C_c on the right-side. The expression is written here again for convenience as (3.10)

$$SR_- = -\frac{I_{ss}}{2C_c} \tag{3.10}$$

The differential slew rate for the first stage is expressed as

$$SR = SR_+ - SR_- = \frac{2I_{ss}}{C_c} \tag{3.11}$$

Comparing the differential output slew rate in (3.6) and (3.10) shows that if the tail current

is boosted by factor of 2, the differential slew rate can also be enhanced by a factor of 2. However, since only extra charging current is provided on one-side compensation capacitor C_c, the enhanced slew rate is non-symmetric as shown in (3.9) and (3.10); the charging side is always faster than the discharging side.

3.3.3 Cascode-Stage Current Boosting

The previous section proposed a method for boosting the tail current during slewing, but it also highlighted the major drawback, i.e., it only provides extra charging current on one compensation capacitor while the discharging current on the opposite side is unchanged, resulting in slew-rate non-symmetry on two sides. The proposed cascode-stage current-boosting method can solve this non-symmetric issue by adding extra discharging transient current. Moreover, the overall differential output slew-rate can be improved further by factor of 3 compared to one without transient current-boosting. The full schematic of the two-stage full-differential folded-cascode op-amp with both tail and cascode-stage current boosting is shown in Figure 3.8.

The cascode-stage current boosting circuit mainly consists of transistors M40-M49 in the bottom red-dashed square in Figure 3.8. M40-M43 replicate dynamic current sources M35-M38 so that the maximum amount of boosted transient current at tail and cascode-stage can be equal and noted as I_{dy}. Transistors M44 and M45 have the same scaled-down size of input pair M1 and M2, that are used to determine to which side the boosted transient current is applied. As shown in Figure 3.8, the large differential signals $(1/2)V_{id}$ and $-(1/2)V_{id}$ are applied at inputs V_{i+} and V_{i-} respectively. As a result, M45 is heavily over-driven while M44 is fully turned off, and all the boosted transient current I_{dy} flows through M45 to discharge node V_{x1} via current mirror M48 and M49. If the large differential signal is applied in an opposite way as in the previous case, the boosted transient current I_{dy} is used to discharge node V_x2. At quiescent and small signal operation, since the dynamic current source M40 and M41 are off, there is no quiescent current flowing in the cascode-stage current boosting circuit. The tail current boosting scheme is the same as that described in the previous section. So the slew rate

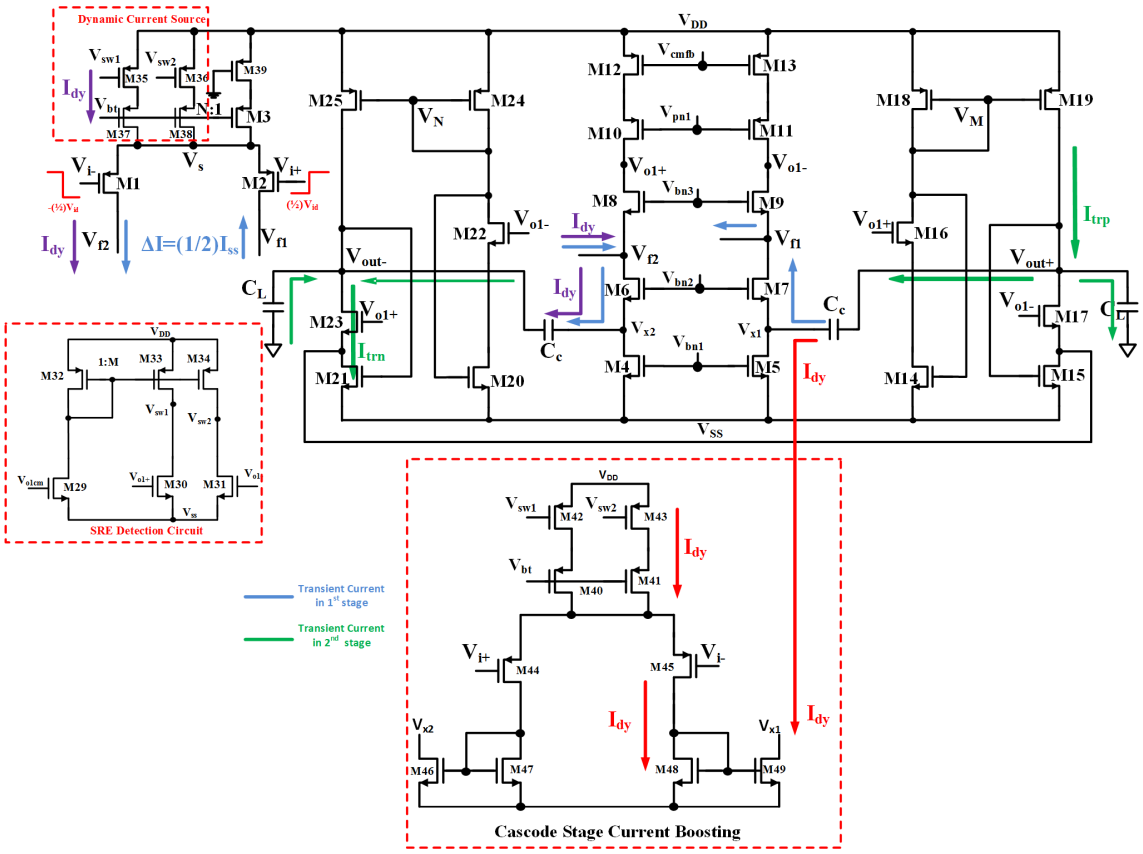

Figure 3.8 Two-stage op-amp with both tail current and cascode-stage current boosting

at V_{o1+} can be expressed as

$$SR_+ = \frac{3I_{ss}/2}{C_c} \tag{3.12}$$

The slew rate at V_{o1-} can expressed as

$$SR_- = \frac{-3I_{ss}/2}{C_c} \tag{3.13}$$

The differential slew rate is expressed as

$$SR = SR_+ - SR_- = \frac{3I_{ss}}{C_c} \tag{3.14}$$

Equation(3.12) and (3.13) show that, with both tail and cascode-stage current boosting, symmetry of charging and discharging slew-rate can be achieved. Moreover, the differential output slew-rate is more enhanced than for the one only boosting the tail current.

3.4 Other Design Consideration

In the previous section, the slew-rate enhancement circuit applied in a two-stage fully-differential folded-cascode op-amp is described in detail. In addition to the SRE scheme, there are two other critical design considerations: common-mode feedback and frequency compensation. In this section, a CMFB circuit and frequency compensation mechanism are described in detail.

3.4.1 Common-Mode Feedback Circuit

One limitation of a fully-differential amplifier is that extra common-mode feedback (CMFB) circuitry is required to fix the common-mode voltage at those high impedance nodes that are not stabilized by negative differential feedback. For the designed op-amp shown in Figure 3.9, since the first stage is a full-differential structure, a CMFB circuit is required to stabilize the common-mode voltage at nodes V_{o+} and V_{o-}. To avoid degrading the gain of the first stage, an active common-mode sensing circuit is used as shown in Figure 3.9 CMFB Circuit 1. The gates of transistors M53 and M54 are both connected to the desired common-mode voltage (V_{ocmref}), and the gates of transistors M52 and M55 are used to sense the common-mode voltage.

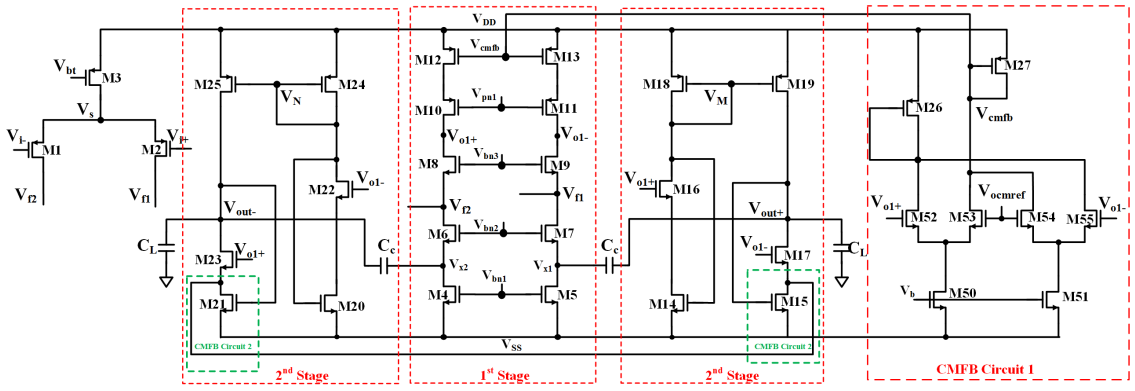

Figure 3.9 Two-stage op-amp with common-mode feedback circuits

Another function of CMFB Circuit 1 is to clearly define the output-stage quiescent current. The drains of transistors M15 and M21 are connected together and they are both operating in the triode region as an output-stage CMFB circuit.

3.4.2 Indirect Frequency Compensation

The traditional compensation technique, well-known as Miller compensation, is to directly feed a compensation current from the output to the internal high-impedance node. Unlikely traditional Miller compensation, indirect compensation, also known as cascode compensation, feeds the compensation current from output nodes indirectly to the internal high-impedance node via another internal low-impedance node. A block diagram of this scheme is shown in Figure 3.10. Compensation capacitor C_c connects output node (2) to internal high-impedance node (1) through the internal low-impedance node B. Figure 3.11 shows the structure of indirect compensation for a two-stage amplifier. The output resistance and the lumped parasitic node capacitance at the outputs of each stage are designated as R_{1-2} and C_{1-2}, respectively. R_B and C_B are the resistance and parasitic capacitance at internal low-impedance node B. C_c is an indirect compensation capacitor forming a feedback network to stabilize the amplifier. C_L is the load capacitor. g_{m1} and g_{m2} comprise the two-stage amplifier. The feedback network is realized by indirect compensation that includes compensation capacitor C_c and a transconductance stage g_{mc}. The indirect compensation scheme removes the RHP zero in conventional Miller compensation by blocking high-frequency feed-forward small-signal current. As mentioned in [17], there are three possible topologies for achieving indirect compensation for a fully-differential two-stage amplifier. The first one is indirect compensation using additional common-stage stage, while the second is indirect compensation using cascoded loads and indirect compensation using cascoded input differential pairs.

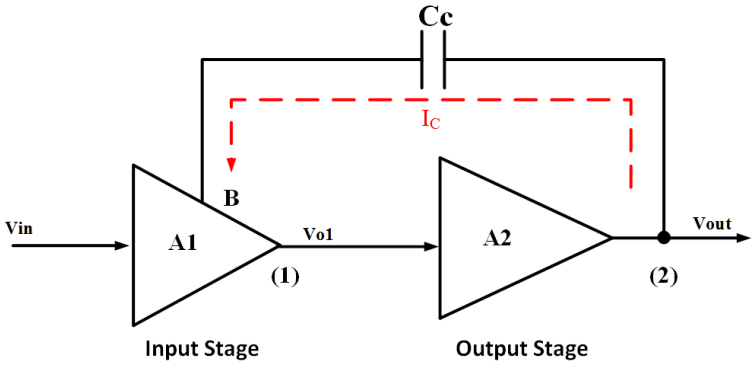

Figure 3.10 Conceptual block diagram of indirect compensation

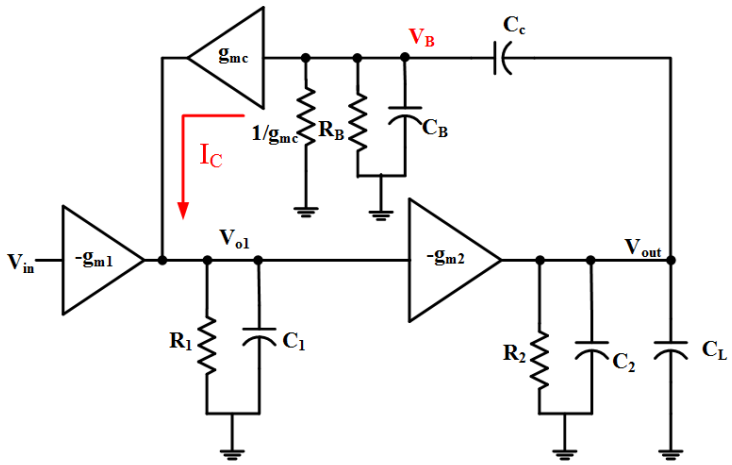

Figure 3.11 Structure of indirect compensation for two-stage op-amp

Figure 3.12 shows the topology of indirect compensation with an additional common-gate stage. The common-gate stage transistors M6 and M7 allow the compensation current to flow from output nodes V_{o+} and V_{o-} to first stage output nodes V_{o1-} and V_{o1+} indirectly while blocking the feed-forward current. In this case, the transconductance g_{mc} in Figure 3.11 corresponds to the transconductance of common-gate transistors M6 and M7. If the transconductance is infinitely large, then the LHP zero can be completely removed and there are only two poles. However, this cannot be true in a practical case; [17] gives a detailed analysis of this topology. The drawback of this topology is that very large extra quiescent current is required to draw on additional common-gate stage transistors M6 and M7 for achieving large transconductance g_{mc}.

To reduce the current consumption in the additional common-gate stage, a cascoded load topology can be used as shown in Figure 3.13. The compensation capacitor connects to the source of load cascode transistors M6 and M7. The resistance at the sources M6 and M7 is approximately of the magnitude of $1/g_{m6}$, i.e, this is a low impedance node. The cascoded load topology can reduce the power and area overhead because the additional common-gate stage is no longer required. However, since transistors M6 and M7 are on the common-mode signal path, the selection of transconductance g_{m6} and g_{m7} is less flexible than when an external common-mode feedback circuit is applied, so the reduction of power and area overhead compared to

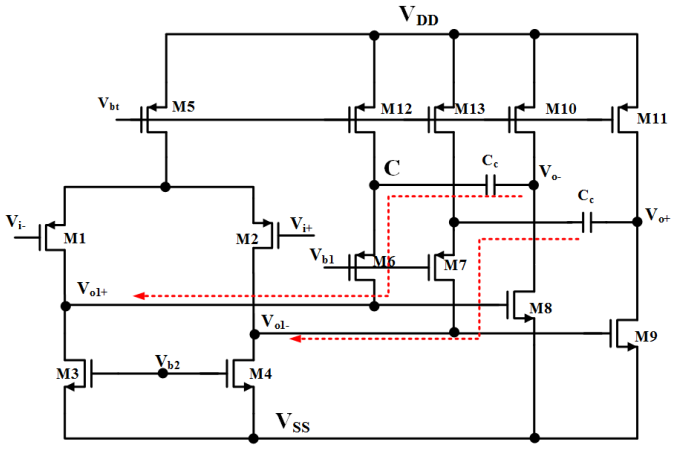

Figure 3.12 Indirect compensation using additional common-gate stage

the additional common-gate stage topology comes at the cost of flexibility in choosing the transconductance g_{mc} that controls the location of the LHP zero.

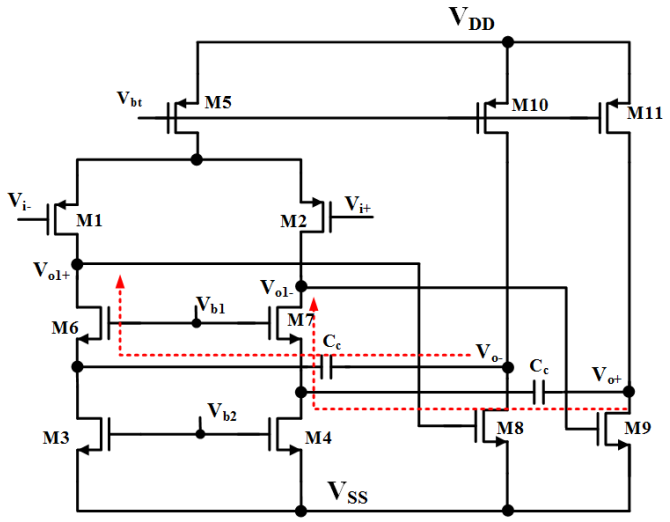

Figure 3.13 Indirect compensation using cascoded load

Alternatively, a cascode differential pair can also be used to indirectly feedback the compensation current. Figure 3.15 shows the implementation of this topology on a telescopic-cascode fully-differential two-stage amplifier. The compensation capacitor connects the source of cascoded input pair transistors M6 and M7. This topology is not, however, the same as for the cascoded load, because the common-gate transistors M6 and M7 are not isolated from the input

pair. This results in a feed-forward current path through the compensation capacitor to the output nodes, and therefore there is an RHP zero.

Although the aforementioned topologies are based on a telescopic structure, they can be extended as well to the folded structure. In this design, the indirect compensation scheme is applied to a folded-cascode structure as shown in Figure 3.5. To prevent the feed-forward current path, the input pair M1 and M2 are folded into cascode stage at nodes V_{f1} and V_{f2}, while the compensation capacitors connect to the sources of load cascode transistors M6 and M7. Another benefit of this configuration is to enhance the transconductance of M6 and M7 by providing a greater quiescent current.

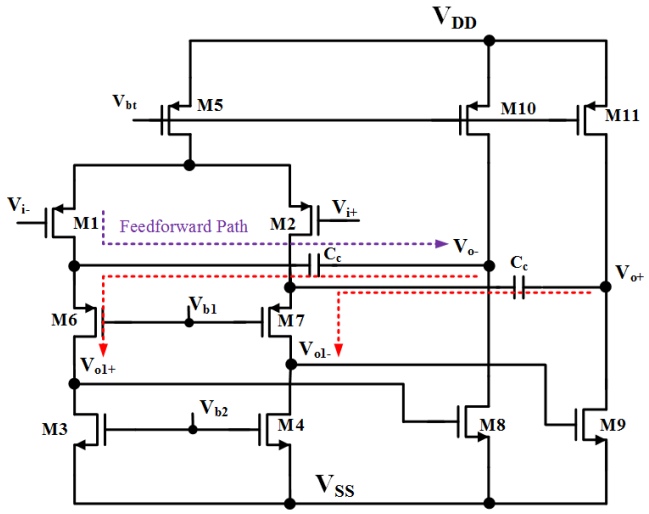

Figure 3.14 Indirect compensation using cascoded input-pair

3.5 Simulation Results

In this section, simulation results are provided that demonstrate the effectiveness of the proposed SRE method. These results also show that the proposed SRE method can preserve the linearity of the core amplifier with respect to total-harmonic-distortion(THD) and AC frequency response.

3.5.1 Large-Signal Step Response

The slew-rate of the designed op-amp was tested in a closed-loop configuration shown in Figure 3.15 in which R_i and R_f comprise the external feedback network. In this case, R_i=R_f=20kΩ. To accommodate the input parasitic capacitor C_{gs}, C_f with a value of 100fF, is placed in parallel with R_f. The external inputs of the amplifier V_i+ and V_i- are biased to the middle of the rail, i.e., V_{ic}=600mV. In this design, V_{DD}=1.2V and V_{SS}=0V.

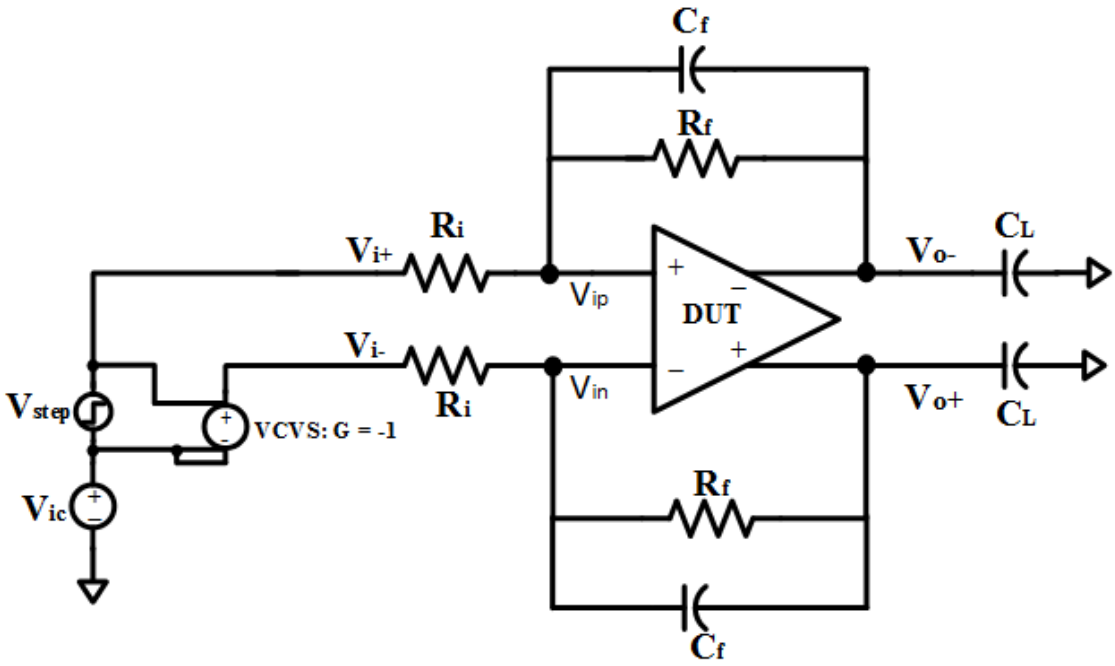

Figure 3.15 Test-bench for slew-rate

The transient responses at single output node V_{o+} and V_{o-} shown in Figure 3.16(a) and Figure 3.16(b), respectively, result from applying a 0.8V step signal to the external input of the amplifier. Both the charging and discharging slew rates are improved by a factor of 2.6. The red and blue curves split at the very beginning of slewing, indicating that the SRE circuit can turn on very fast. Without such slew-rate enhancement (the blue curve in Figure 3.16(a) and Figure 3.16(b)), the positive slew rate is 16V/μs and the negative slew rate is 15V/μs; with slew-rate enhancement (the red curve in Figure 3.16(a) and Figure 3.16(b)), the positive slew rate is 41V/μs and the negative slew rate is 41V/μs.

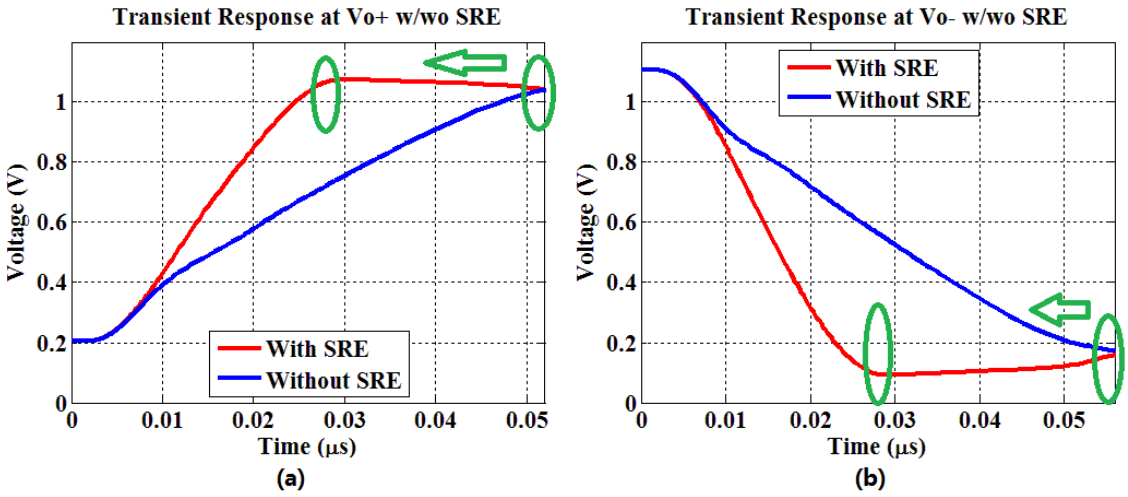

Figure 3.16 (a)transient response at V_{o+} (b)transient response at V_{o-}

The transient response of the differential output is shown in Figure 3.17. The blue curve corresponds to the one without SRE circuit, while the red curve is the one with SRE circuit. The differential output slew rate is improved from 31V/μs to 82/Vμs and the SR is improved by a factor of 2.6.

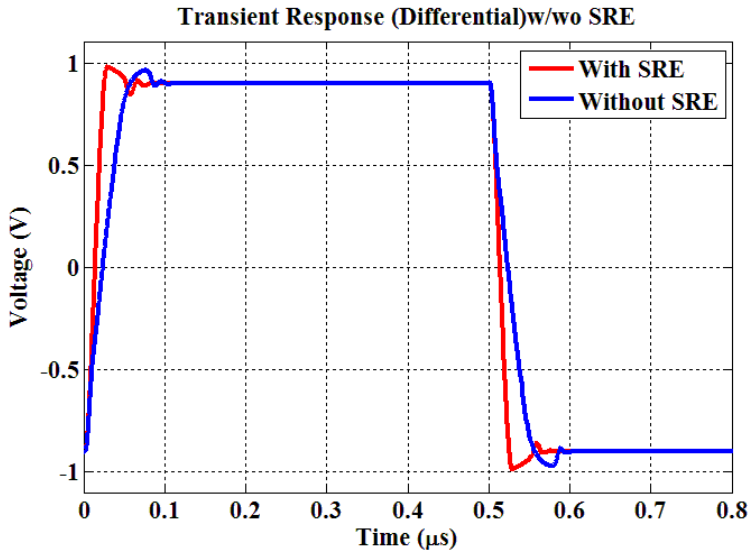

Figure 3.17 Transient response at $V_{o+} - V_{o-}$

To verify the robustness of the SRE method, process corners and temperature simulation were also performed. Figure 3.18 shows the simulation results both with and without the

proposed SRE method. The solid curves represent those representing the proposed SRE scheme while the dash lines corresponds to those without SRE scheme. The simulation results indicate that with the proposed SRE method the differential SR can be enhanced by a factor of at least 2.2 over all the process corners and a temperature range from 0 °C to 60 °C.

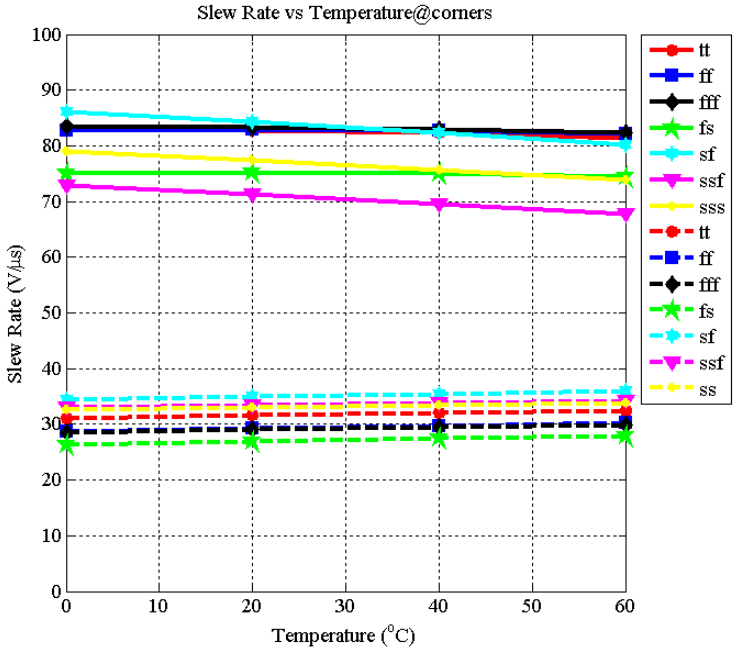

Figure 3.18 SR with/without SRE with temperature variation at different process corners

Theoretically, as shown in the analysis of the previous section, by doubling the tail current the differential slew rate can be enhanced by factor of 3. However, as shown in Figure 3.18, the simulated differential slew rate with SRE circuit is improved by factor of 2.2 compared to the one without the SRE. The reason is that the tail current during slewing is boosted by only a factor of 1.8 instead of 2, as shown in Figure 3.19.

3.5.2 Small-Signal Step Response

The small-signal step response of the amplifier was simulated using the test-bench shown in Figure 3.15. Upon applying a small step signal V_{step}=100mV to the external inputs, the differential output settles as shown in Figure 3.20. The small-signal settling curve retains the same shape regardless both with and without SRE circuit, indicating that the SRE circuit is

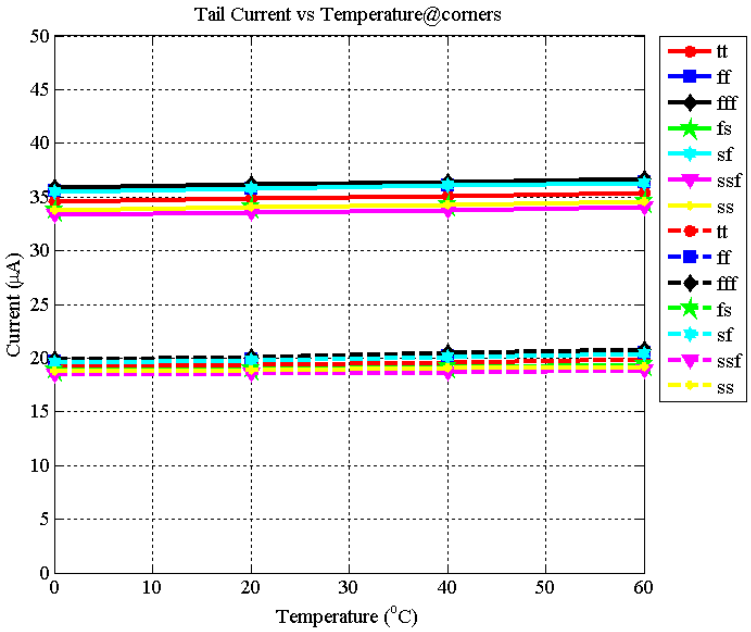

Figure 3.19 Tail current during slewing with/without SRE

inactive for small-signal operation. The amplifier with SRE has 8.53% overshoot and requires 33.57ns for 1% settling, while the one without SRE has 7.68% overshoot and requires 32.84ns for 1%settling.

3.5.3 AC Frequency Response

The AC frequency response of the op-amp was simulated using the same test-bench shown in Figure 3.15. The only difference in this case is that a sinusoidal input with 100mV peak-to-peak value was applied as the differential input instead of a step signal. By performing stability analysis in the simulator, loop stability can be verified in terms of phase margin of loop transfer function $A\beta$. The loop transfer function is written as (3.15) and the simulated bode plot for both with and without SRE are in Figure 3.5.

$$LoopGain = A\beta = \frac{V_{o+} - V_{o-}}{V_{ip} - V_{in}} \frac{R_i||C_{ip}}{R_i||C_{ip} + R_f||C_f} \tag{3.15}$$

where A is the open-loop gain of the amplifier, β is the external feedback factor and C_{ip} is the lumped parasitic capacitor at the gate of input differential pair.

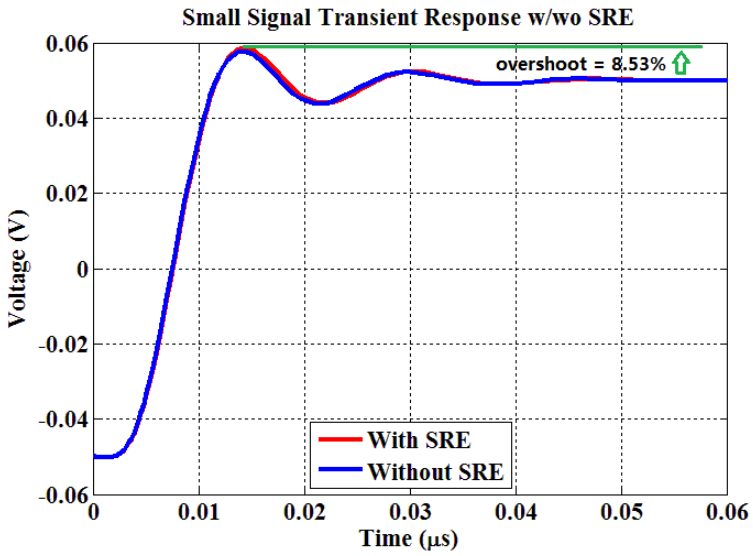

Figure 3.20 Small-signal step response

As shown in the Bode plot of Figure 3.21, the loop frequency response for the amplifiers both with SRE and without SRE are exactly the same. The loop gain is 76 dB, the Gain-Bandwidth-Product(GBW) is 30.48MHz, the Unity-Gain frequency is 35.21MHz and the phase margin is 60.15°.

The open-loop frequency response can also be simulated as shown in Figure 3.22. The red curve (with SRE) and blue curve (without SRE) are exactly the same. The open-loop gain for the amplifier both with and without SRE is 82dB. The GBW and UGF are 61.81MHz and 64.99MHz, respectively; thus, from the AC frequency response perspective, the proposed SRE method has no impact on the small-signal performance of the core amplifier.

3.5.4 Linearity

The linearity can be represented in terms of total harmonic distortion(THD). By applying a sinusoidal signal at the input and performing a Discrete Fourier Transform(DFT) for the differential output signal, the THD of the amplifier for different input sinusoidal signal levels at various frequencies can easily be obtained. To verify that the proposed SRE method can preserve the linearity of the core amplifier, the THD of the amplifier with and without SRE were obtained for different sinusoidal input signal peak-to-peak values and frequencies. The

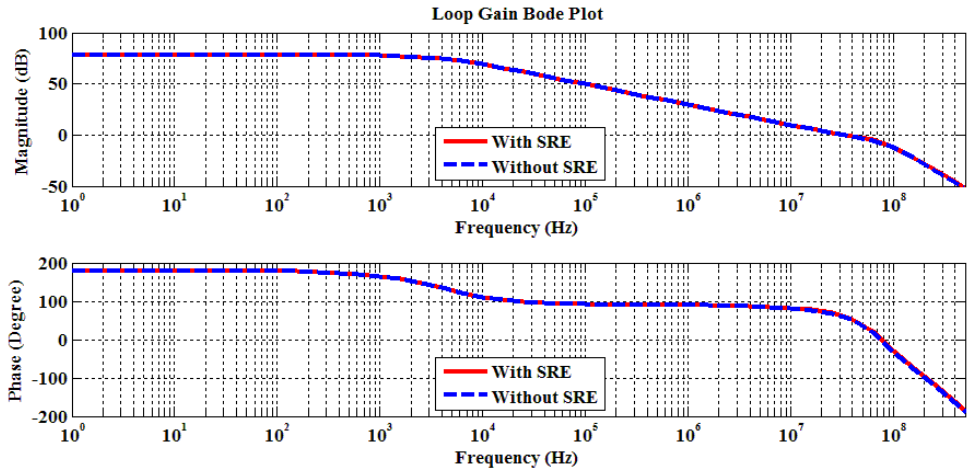

Figure 3.21 Loop gain bode plot

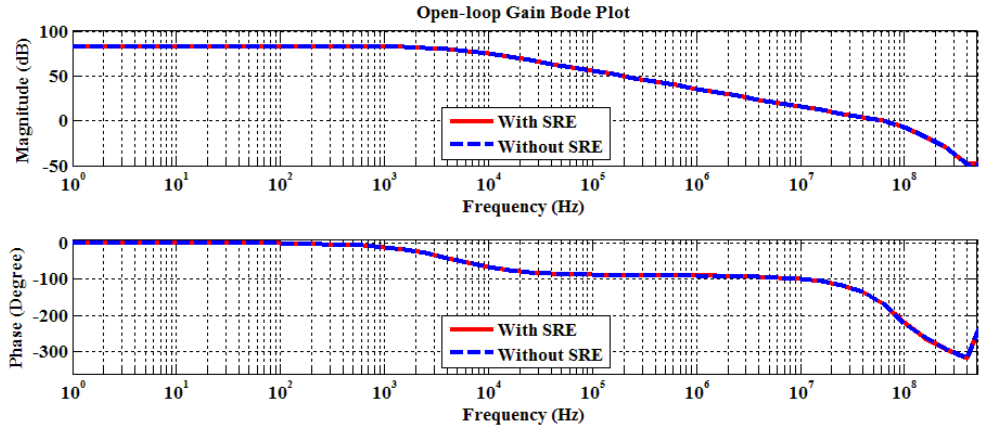

Figure 3.22 Open-loop gain bode plot

test-bench used for this simulation was exactly the same as the one shown in Figure 3.15. Table 3.2 shows the simulation results. In the table, columns correspond to different input sinusoidal frequencies and rows correspond to different peak-to-peak values. Each cell in the table includes two numbers; the left one is the THD with SRE and the right one is the THD without SRE.

The simulation results indicate that the THD of the amplifier can be preserved at its original level with the proposed SRE method. In other words, the linearity of the amplifier will not be degraded when applying the proposed SRE circuit. However, as for the design in [7], the adaptive biasing method can degrade the THD 12dBc with 0.6V V_{pp} at a 1MHz frequency.

Table 3.2 THD of amplifier with/without SRE at different input sinusoidal signal magnitude and frequency(Unit: dBc)

Vpp/Freq	10kHz(w/wo)	100kHz(w/wo)	1MHz(w/wo)	5MHz(w/wo)
0.1V	-166.32/-166.86	-150.73/-150.01	-114.81/-114.83	-77.01/-77.09
0.2V	-154.29/-154.84	-139.12/-139.18	-104.28/-104.68	-65.36/-65.47
0.3V	-147.89/-147.18	-132.32/-132.70	-98.06/-98.59	-57.88/-57.99
0.4V	-141.21/-141.13	-128.63/-128.36	-93.33/-93.93	-52.03/-52.15
0.5V	-135.17/-135.67	-125.23/-125.45	-90.13/-90.63	-46.72/-46.91
0.6V	-130.02/-130.12	-123.56/-123.89	-86.63/-86.37	-41.48/-40.62

3.6 Layout

This prototype design was implemented in IBM 130nm process and fabricated through the MOSIS research program. Matching is critical in analog circuit design, and op-amps require particularly high matching performance for achieving small input-referred offset and high common-mode rejection ratio. Such transistor matching is mainly dependent on transistor size, transistor shape, and transistor orientation [17]. Transistors with large gate areas generally have better matching performance than those with small gate area, because as WL increases, localized random variation can be averaged out more effectively. Transistors with larger channel lengths achieve better matching than short channel transistors since the channel length effect can be significantly reduced. Transistors with identical gate orientations have better matching performance than those with different directions. In this design, transistor length was chosen to be 600nm and all the transistors gates had the same orientation. In addition, wider transistors were laid out using multi-finger transistors to reduce both S/D junction area and gate resistance. Symmetry is also important for a fully-differential amplifier, so all the stages of this amplifier were laid out symmetrically. A two-dimensional common-centroid layout technique was applied to the input-pair transistors for the purpose of eliminating first-order gradient effects in both X-axis and Y-axis directions, while all other parts were laid out using a one-dimensional common-centroid. The floor planning of the amplifier layout is shown in Figure 3.23 and the layout is shown in Figure 3.24.

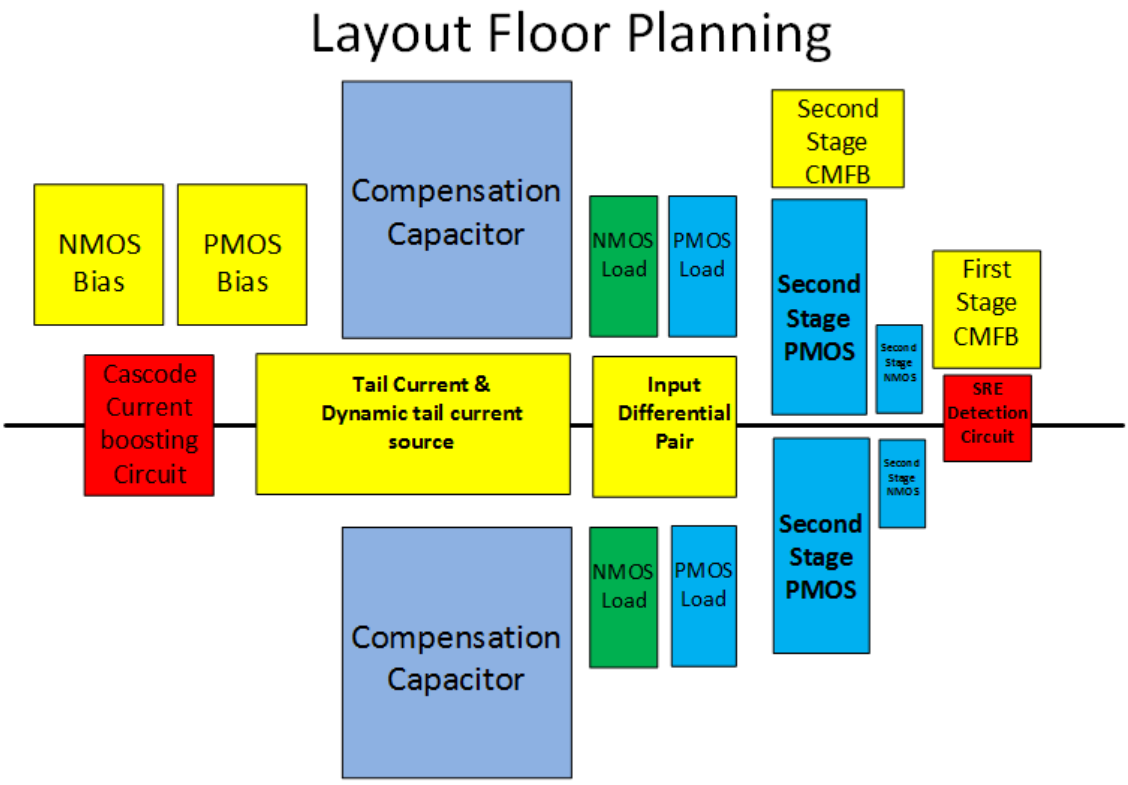

Figure 3.23 Op-amp Layout Floor Planning

3.7 Op-amp Performance Summary

The performance of the two designed amplifiers is summarized and compared in Table 3.3. The small-signal performance was well-preserved in terms of AC performance. The settling time was reduced by 30%, since with SRE the op-amp has less time in slewing. The total current consumption is small and area overhead was only 2.22%.

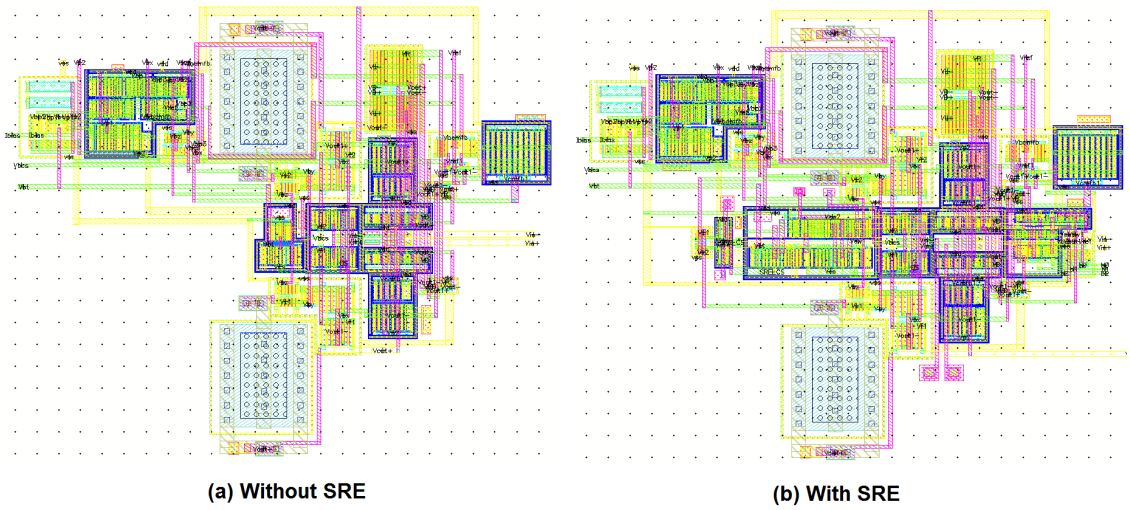

Figure 3.24 Layout of full-differential op-amp (a) without proposed SRE circuit (b) with proposed SRE circuit

Table 3.3 Performance summary of two designed op-amps

Specs	**Without SRE**	**With SRE**
Technology	IBM 130nm	
Supply Voltage (V)	1.2	1.2
Load Capacitor (pF)	20	20
Open Loop DC Gain (dB)	82.47	82.47
Open Loop GBW (MHz)	61.81	61.81
Open Loop UGF (MHz)	64.99	64.99
Phase Margin (Deg)	60.15	60.15
Slew Rate (MV/s)	33.43	82.23
1% Settling Time (ns)@ 0.9V Step Input	98.29	69.61
THD(dBc)@ Vpp=0.6V Freq=5MHz	-40.62	-41.48
Current Consumption(μA)	150	170
Area (μm^2)	6300	6440

CHAPTER 4. SLEW RATE ENHANCEMENT CIRCUIT INDUCED TROJAN STATE, THEIR DETECTION AND REMOVAL

4.1 Introduction

It is well-known that many analog building blocks such as self-stabilized generators, voltage and current references, and frequency references are vulnerable to multiple operating points problem. Such undesired operating points (also known as "Trojan state") can result in circuits failing to operate as desired. The fully differential op-amp, a fundamental active element employed in modern analog and mixed-signal systems such as data converters and filters, can also suffer from such Trojan state problem when they are designed using performance enhancement feedback. In particular, the slew rate enhancement (SRE) method is one of the most widely-used performance enhancement techniques in low-power high-speed op-amp design [3] [5] [7] [8] [9], but most of these methods are either incompatible with low-voltage operation [8], have degraded linearity [3] [5], or increase circuit complexity [9]. Recently, the SRE method described in [7] has offered a simpler and more power and area-efficient method based on excessive transient detection to enhance slew rate while preserving small-signal performance and improving linearity. However, since this method is based on sensing internal nodes of the amplifier to control dynamic current source, an associated positive feedback loop (called "SRE loop") is inevitably introduced.

Recently, several efficient analog verification methods have been proposed in the literature [13] [14] [15] [16] to identify and break positive feedback loops (PFL) as well as to detect all Trojan states in analog circuits. Generally speaking, the process of detection and removal of Trojan states in op-amp can be divided into three steps: (a) identifying positive feedback loops in op-amps and determining break-points of these PFLs, (b) finding all the Trojan states in

op-amp, and (c) modifying the circuit to remove all Trojan states. For step (a), the loop identification method in [14] [15] can be used to automatically identify and break PFLs. Following that, either the break-loop homotopy method discussed in [13] or the divide and contraction verification method described in [16] can be using in step (b) to find all the Trojan states. In step (c), modifications must be performed on the original circuit to block DC signal paths in PFLs so that Trojan states can be removed.

In this chapter, we first show that using a performance enhancement circuit can result in the presence of Trojan states in fully-differential op-amps. In particular, an SRE circuit as described in [7], together with widely-used two-stage op-amp, is taken as an example to illustrate this phenomenon and demonstrate our analysis result. Subsequently, a systematic method for identifying and removing Trojan states in this example circuit is proposed. Simulation results will also be provided to demonstrate the effectiveness of this approach. This new SRE circuit represents design of a fully-differential class AB op-amp and the simulation results indicate that the circuit can provide the desired function while removing all Trojan states.

This chapter is organized as follows. In Section 4.2, Trojan states resulted from performance enhancement feedback is analyzed and demonstrated through an example. A systematic detection, removal and verification method is proposed in Section 4.3. In Section 4.4, using the proposed Trojan state removal method, a fully differential class AB op-amp is designed and simulation results are provided. Section 4.5 briefly concludes this work.

4.2 Trojan State Unveiled in Performance-Enhancement Feedback

Similarly to the well-known self-stabilized circuit, a fully-differential op-amp with performance enhancement circuitry also can suffer from a Trojan state problem. The conceptual block diagram of a half equivalent circuit for a balanced fully-differential amplifier is shown in Figure 4.1. Loop 1 is an external feedback network and as such as often defined by a specific application. Loop 2 is a strong negative feedback path, known as a common-mode feedback loop, and used to stabilize the op-amp's common-mode voltage. The performance enhancement circuit, shown as loop 3 in Figure 4.1 , senses the voltage or current signal at internal nodes of the op-amp and dynamically controls an circuit added for feeding back to some internal point in

the op-amp. This operational principal can inevitably introduce positive feedback loops, often resulting in the presence of a Trojan state. In particular, the SRE circuit is widely used in low-power high-speed op-amp design. The method proposed in [7] can achieve better performance than other proposed SRE methods in terms of power and area overhead and circuit complexity. As demonstrated in [7], this SRE method can improve slew rate and total harmonic distortion by factor of 23.2 and 6dB respectively with only 2% power and 1.2% area overhead. However, when applying this SRE circuit to a fully-differential op-amp, it turns out that the circuit can be stuck into an undesired stable DC operating point.

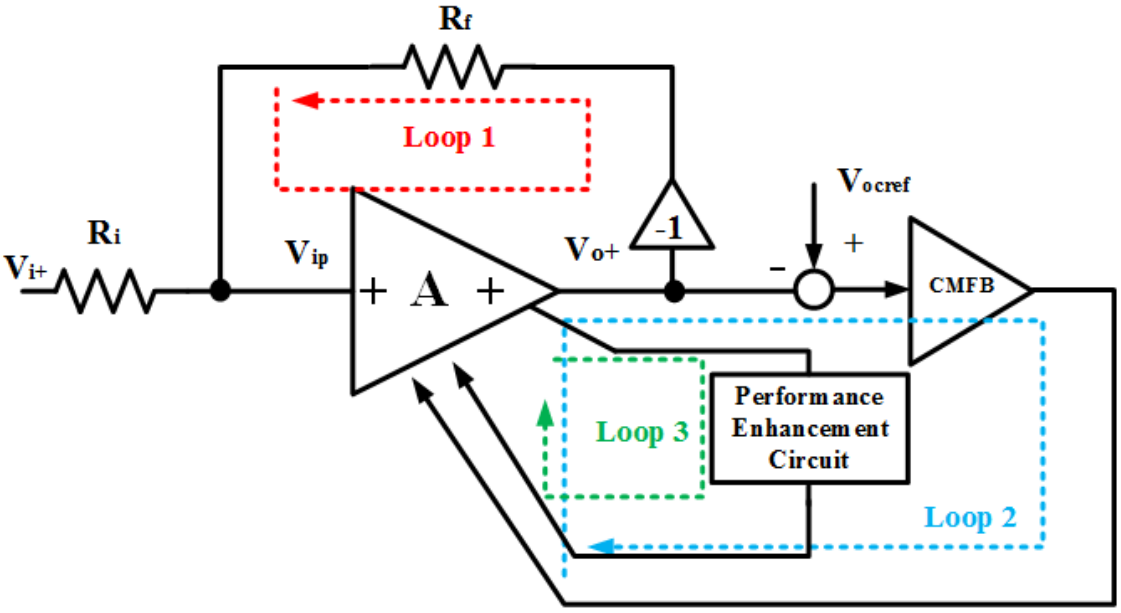

Figure 4.1 Conceptual block diagram of fully-differential op-amp with performance enhancement circuit

4.2.1 PFL Due to SRE Circuit

The SRE circuit proposed in [7], and shown in Figure 4.2, consists of a slew-rate detection circuit M29-M31 and a dynamic current source M28 with its associated switch M34. The gates of M30 and M31 are connected to the internal nodes of op-amp V_{o1+} and V_{o1-} respectively, and the gate of M29 is biased to the common-mode voltage of the two nodes. M29 - M31 have the same widths and lengths. The current-mirror ratio M is set to be larger than two so that

M33 operates in the triode region at DC. As a result, V_{sw} is near V_{DD} to turn off the dynamic current source M28. During slewing, when a large complementary signal is sensed by M30 and M31, the total current in them will dramatically increase, resulting in V_{sw} decreasing and ultimately approaching V_{SS} to fully turn on M28. However, as in the operation of the SRE circuit described above, the transfer function from V_{o1+} and V_{o1-} to V_s has a positive slope. If in the amplifier core the transfer function from V_s to V_{o1+} and V_{o1-} also has a positive slope, then the loop formed due to the SRE circuit will be a positive feedback loop. Unfortunately, this is the actual situation because slewing is often sensed at the input stage's output nodes and the dynamic current source is connected into the amplifier core at the common-source node of the input differential pair.

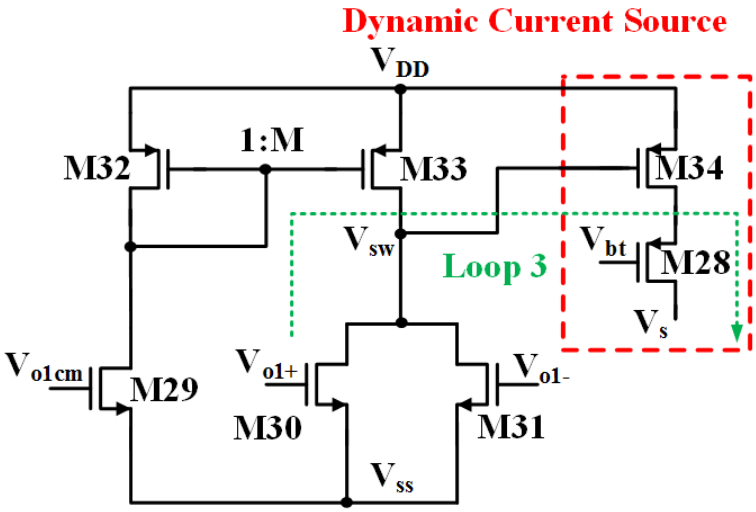

Figure 4.2 SRE circuit proposed in [7]

4.2.2 Two-Stage Op-amp Example

To illustrate the PFL due to the previously-discussed SRE circuit, a class AB two-stage op-amp, as shown in Figure 4.3, was designed using an SRE circuit as in [7]. The two-stage op-amp has a folded-cascode input stage followed by a class AB output stage. To achieve higher speed with a certain power consumption, cascode compensation [18] was applied. A CMFB circuit was used to stabilize the input stage common-mode voltage by using a feedback voltage to bias M12 and M13. In addition, M15 was used to stabilize the class AB output stage common-mode

voltage. Without the SRE circuit in Figure 4.2, upon running DC analysis in the simulator, the op-amp operates properly at the desired DC operating point. However, once the SRE circuit is added as in Figure 4.2, the op-amp will become stuck at an incorrect DC operating point. The desired and undesired DC operating points at nodes V_{o1+} and V_{o1-} are listed in Table 4.1. Theoretically, at DC the SRE circuit will always be off as long as the current-mirror ratio $M > 2$, since in this case M33 is operating in the triode region. However, because of the SRE circuit induced PFL as discussed earlier, there is another stable DC operating point at which V_{o1+} and V_{o1-} are both stuck at 1.2V (V_{DD}) and V_{sw} is near to V_{SS}.

Table 4.1 DC operating points at V_{o1+} and V_{o1-}

Simulation	**Node Voltage**
Without SRE (Desired)	486 mV
With SRE (Undesired)	1.2V

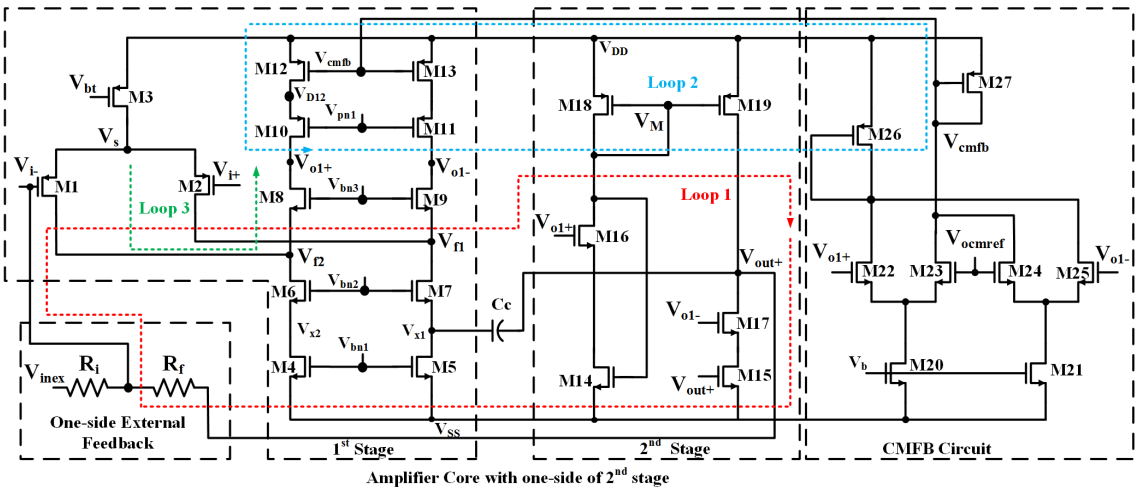

Figure 4.3 Two-stage fully-differential class AB op-amp

4.3 Systematic Detection, Removal and Verification

In this section, we will propose the method to systematically detect and remove Trojan states induced by performance enhancement circuitry in op-amp. In particular, modification

will be performed on the SRE circuit from [7] to remove the induced PFL while keep its effectiveness on enhancing slew rate.

4.3.1 Review of Analog Verification Method Against Trojan State

Recently, several efficient analog verification methods been proposed in the literature [13] [14] [15] [16]. The method proposed in [14] [15] uses a graphical method to detect PFLs and determines a break-point. It first converts the circuit netlist into a directed dependency graph (DDG) and then partitions the DDG into strongly connected components (SCC). By employing graph theory, all the PFLs can be easily detected and the break-point located for each SCC. The advantage of this method is that it can identify all the PFLs based solely on the circuit structure rather than by computing DC solutions. With respect to finding Trojan states, in [13] the break-loop homotopy method is discussed in detail. This method needs first to break all positive feedback loops in the circuit and then simultaneously insert a swept signal source at all break-points to find stable operating points. To overcome the low efficiency of the homotopy method, a monotonic divide and contraction based method is proposed in [16]. This method targets finding voltage intervals containing undesired stable operating points rather than finding all operating points or even any operating point at all; this is the reason why this method could be more efficient than the conventional break-loop homotopy method.

4.3.2 Identification and Break of PFLs

By applying the break-loop method in [14] [15] and using a half-equivalent circuit approach as shown in Figure 4.1, three feedback loops are found in the two-stage op-amp with an SRE circuit, as shown in Figure 4.2 & Figure 4.3

Loop 1: $V_{out+} \rightarrow V_{i-} \rightarrow V_{f2} \rightarrow V_{o1+} \rightarrow V_M \rightarrow V_{out+}$ (positive)

Loop 2: $V_{o1+} \rightarrow V_{cmfb} \rightarrow V_{D12} \rightarrow V_{o1+}$ (negative)

Loop 3: $V_{o1+} \rightarrow V_{sw} \rightarrow V_S \rightarrow V_{f2} \rightarrow V_{o1+}$ (positive)

Loop 1 is the external feedback loop (Figure 4.3); Loop 2 is the CMFB loop (Figure 4.3), and Loop 3 is the SRE feedback loop (Figure 4.2 & Figure 4.3). The break-point for simultaneously breaking all the positive feedback loops can be only at node V_{o1+}. However, breaking all the

PFLs at node V_{o1+} also results in cutting off the negative feedback loop, leading to the return map being non-monotonic. The return map is defined in [16]; it represents the transfer function from the break-point around the loop back to the break-point. At break-point V_{o1+}, a variable voltage source $V_{in} = x$ is applied, and by performing a linear sweep of x in the range from V_{SS} to V_{DD}, the return map $f(x)$ is generated. The operating points are then where $f(x) = x$. As shown in the simulated return map in Figure 4.4, three DC operating points are present. According to a Theorem proven in [16], the DC operating points corresponding to point A and C are stable DC operating points and point B is an unstable one. Obviously, point A is the desired operating point while point C is an undesired operating point, consistent with the DC analysis simulation results listed in Table I.

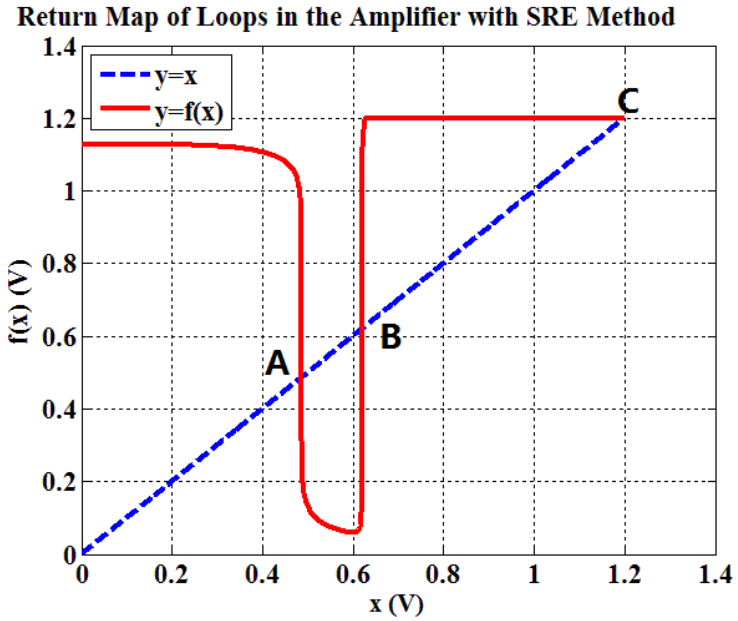

Figure 4.4 Return map of loops in the op-amp with SRE method from [7]

4.3.3 Proposed Method for Removal of Trojan State

To break the PFL, a new SRE circuit is proposed in Figure 4.5. With a few modifications of the SRE circuit in [7], it not only completely breaks the PFL at DC to remove the undesired DC operating points, but also retains effectiveness in detection of slewing. The principle of breaking the loop is to insert a DC blocking capacitor between the drains of differential pair

M30 and M31 and the dynamic current source control voltage V_{sw}. As a result, the positive feedback loop is broken at node D30 and V_{sw} is exactly equal to V_{DD} at DC for fully turning off the dynamic current source. Moreover, to turn on the dynamic current source during slewing, V_{sw} must be discharged near V_{SS} instantaneously. To achieve this, node $D30$ is precharged near V_{DD} at DC via M33B. This requires M33B to be in triode region at the DC operating point, so the current mirror (M33B and M32) ratio M is set to be larger than 2. During slewing, since the total current in M30 and M31 significantly increases, node D30 is discharged near V_{SS} so that node S33 is also discharged and V_{sw} finally approximates V_{SS} to fully turn on the dynamic current source.

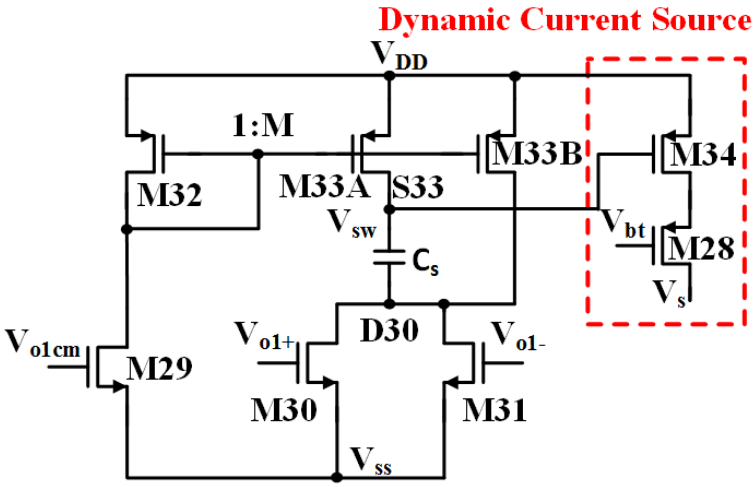

Figure 4.5 Proposed SRE circuit

4.4 Design Example and Simulation Results

The circuit shown in Figure 4.3, together with the proposed SRE circuit in Figure 4.5, was implemented in IBM 0.13-μm technology with a supply voltage ranging from 0 to 1.2V. Dynamic current source M28 in Figure 4.5 is sized with ratio of 3 with respect to tail current source M3 so that the maximum boosted tail current is 3 times the static tail current. As a result, the slew rate can be enhanced by a factor of 3. To verify the effectiveness of removing Trojan states in the op-amp, the loop identification method can be applied to the designed op-amp. The following two loops are found.

Loop 1: $V_{out+} \rightarrow V_{i-} \rightarrow V_{f2} \rightarrow V_{o1+} \rightarrow V_M \rightarrow V_{out+}$ (positive)

Loop 2: $V_{o1+} \rightarrow V_{cmfb} \rightarrow V_{D12} \rightarrow V_{o1+}$ (negative)

The break-point is at V_{o1+}, as determined by the loop identification method. Next, the break-loop homotopy method can be used to generate the return map as shown in Figure 4.6. Although the positive and negative feedback loops simultaneously exist, the negative feedback (common-mode feedback) loop is much stronger than the positive external feedback loop (as shown in Figure 4.3), always leading to an overall return map with negative slope. As a result, there is a unique stable DC operating point, exactly the same as for the one without the SRE circuit shown in Table I.

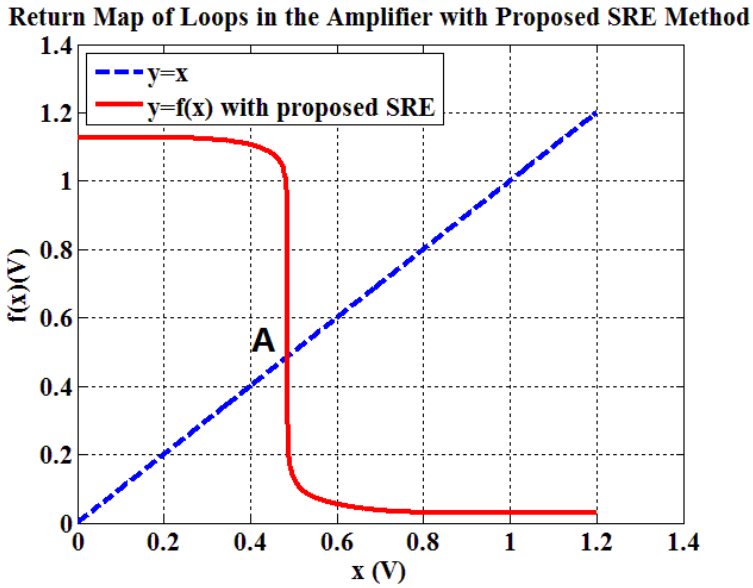

Figure 4.6 Return map of loops in op-amp with proposed SRE circuit

4.5 Conclusion

In this chapter, we show that Trojan states can be introduced into an op-amp when a performance enhancement circuit is incorporated. In particular, a SRE circuit has been taken as an example to investigate this Trojan state problem. To deal with this problem, a systematic method of identifying and removing Trojan states has been proposed and its effectiveness demonstrated using this SRE circuit example. In general, to remove the Trojan states intro-

duced by the large-signal performance enhancement circuit, we must modify the enhancement circuit to guarantee that the loop formed only responses to large-signal while being blocked at DC.

CHAPTER 5. CONCLUSION AND FUTURE RESEARCH

With the rapid pace of reducing CMOS transistor feature size, the supply voltage is correspondingly scaled down to ensure device reliability and low-power consumption on single VLSI cells. As a result, op-amp design becomes more challenging because its performance is significantly degraded in terms of factors like SR, DC gain, noise, SNR, swing range and linearity. During the most recent two decades, many performance-enhancement circuits have been proposed in the literature to accommodate this CMOS evolution as predicted by Moore's Law. These performance enhancement circuits can be divided into three categories: DC performance enhancement, small-signal AC/transient performance enhancement, and large-signal transient performance enhancement. In this thesis, a novel slew-rate enhancement method based on excess transient detection and feedback is presented. In Chapter 2, the basic concept of a proposed SRE technique using excess transient feedback is described, and then a circuit implementation of such a SRE circuit is provided along with a detailed quantitative analysis. Compared to the previously reported SRE method, the proposed SRE method has the advantage of having pre-defined turn-on voltage, fast detection of slewing, and preserving small-signal performance and linearity of the core amplifier. In Chapter 3, a two-stage folded-cascode fully-differential amplifier was designed employing the proposed slew-rate enhancement technique in IBM 130nm process. Large-signal transient analysis was performed on this proposed op-amp to demonstrate its effectiveness in terms of improving slew rate symmetrically. Chapter 4 illustrates that an SRE circuit can induce undesired operating points (also known as"Trojan states") as an op-amp issue. For such circuits, a systematic method for detecting and removing Trojan states is presented. Using a design example and simulation results, it is demonstrated that the proposed method can effectively remove Trojan states in the op-amp while preserving the effectiveness of improving slew-rate.

The simulation results have shown the effectiveness of the proposed method on improving slew-rate while preserving the linearity of the amplifier. However, silicon measurement results are also required to further demonstrate true feasibility. Thus, a fabricated chip of the fully-differential two-stage amplifier will be tested in the lab. A Printed-Circuit-Board(PCB) will be designed to carry out this op-amp measurement, and in addition, further improvement of this SRE method will be performed to simultaneously alleviate both internal slew rate and output stage slew rate limitations. With these improvements in the SRE method, another op-amp will be designed to demonstrate its expected improved performance with respect to slew-rate.

BIBLIOGRAPHY

[1] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS, "*IEEE J. Solid-State Circuits*,vol 40, pp. 132-143,Jan. 2005

[2] B. Huang, D.G. Chen "A high gain operational amplifier via an efficient conductance cancellation technique, "*in Proc. IEEE Custom Integrated Circuit Conference*, pp.1-4, Sep.2014

[3] M. Degranuwe, J.Rijmenants, E.A.Vittoz, and D.Man,"Adaptive biasing CMOS amplifiers, "*IEEE J. Solid-State Circuits*,vol.SC-17,pp522–528, Jun 1982

[4] A.P Perez, N.K Y.B, E. Bonizzoni, and F. Maloberti,"Slew-Rate and Gain Enhancement in Two Stage Operational Amplifiers ,"*in Proc. IEEE Int. Symp. Circuits Systems*, pp. 2485-2488 May 2009

[5] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R.G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency,"*IEEE J. Solid-State Circuits*,vol.40, no.5, pp.1068–1077, May 2005

[6] B. Huang, L. Xu, D.G. Chen, "Slew rate enhancement via excessive transient feedback,"*Electronics Letters*, pp.930-932, July 2013

[7] B. Huang, D.G. Chen, "A simple slew rate enhancement technique with improved linearity and preserved small signal performance,"*in Proc. IEEE MWSCAS*, pp.270–273, Aug. 2014

[8] B.W. Lee, and B.J Sheu, "A high slew-rate CMOS amplifier for analog signal processing,"*IEEE J. Solid-State Circuits*, vol.25, no.3, pp.885–889, June 1990

[9] R. Harjani, R. Heineke, and F. Wang, "An integrated low voltage class AB CMOS OTA," *IEEE J. Solid-State Circuits*, vol.34, no.2, pp.134–142, Feb 1999

[10] J. Karki, "Fully Differential amplifier," *Texas Instruments Application Report*, Jan. 2002

[11] P.E Allen, D.R Holberg, "CMOS Analog Circuit Design," *OXFORD UNIVERSITY PRESS*, Second Edition

[12] J.N. Babanezhad, "A rail-to-rail CMOS op amp," *IEEE J. Solid-State Circuits*, vol.23, no.6, pp.1414-1417, Dec 1988

[13] Y.-T. Wang, D.G. Chen, R. L. Geiger, "Practical methods for verifying removal of Trojan Stable Operating points," *in Proc. IEEE Int. Symp. Circuits Systems*, pp. 2658–2661 May 2013

[14] Z.Q. Liu, Y. LI, R. L. Geiger, D. G. Chen, "Auto-identification of Positive Feedback Loops in Muti-state Vulnerable Circuits," *VSLI Test Symposium (VTS)*, pp. 1–5, April 2014

[15] Z. Q. Liu, Y. LI, Y. DUAN, R. L. Geiger, D. G. Chen, "Identification and break of positive feedback loops in Trojan States Vulnerable Circuits," *in Proc. IEEE Int. Symp. Circuits Systems*, pp. 289–292, June 2014

[16] Y. Li; D. G. Chen, "Efficient analog verification against Trojan State using divide and contraction method," *in Proc. IEEE Int. Symp. Circuits Systems*, pp. 281-284, June 2014

[17] Kumar, Vaibhav, "High bandwidth low power operational amplifier design and compensation technique,"*Graduate Theses and Dissertations*, Paper 10766,2009

[18] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers,"*IEEE J. Solid-State Circuits*,vol. 18, no. 6, pp.629–633, Dec. 1983